

Compal Confidential

NAWF2 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M+M92-S2 XT

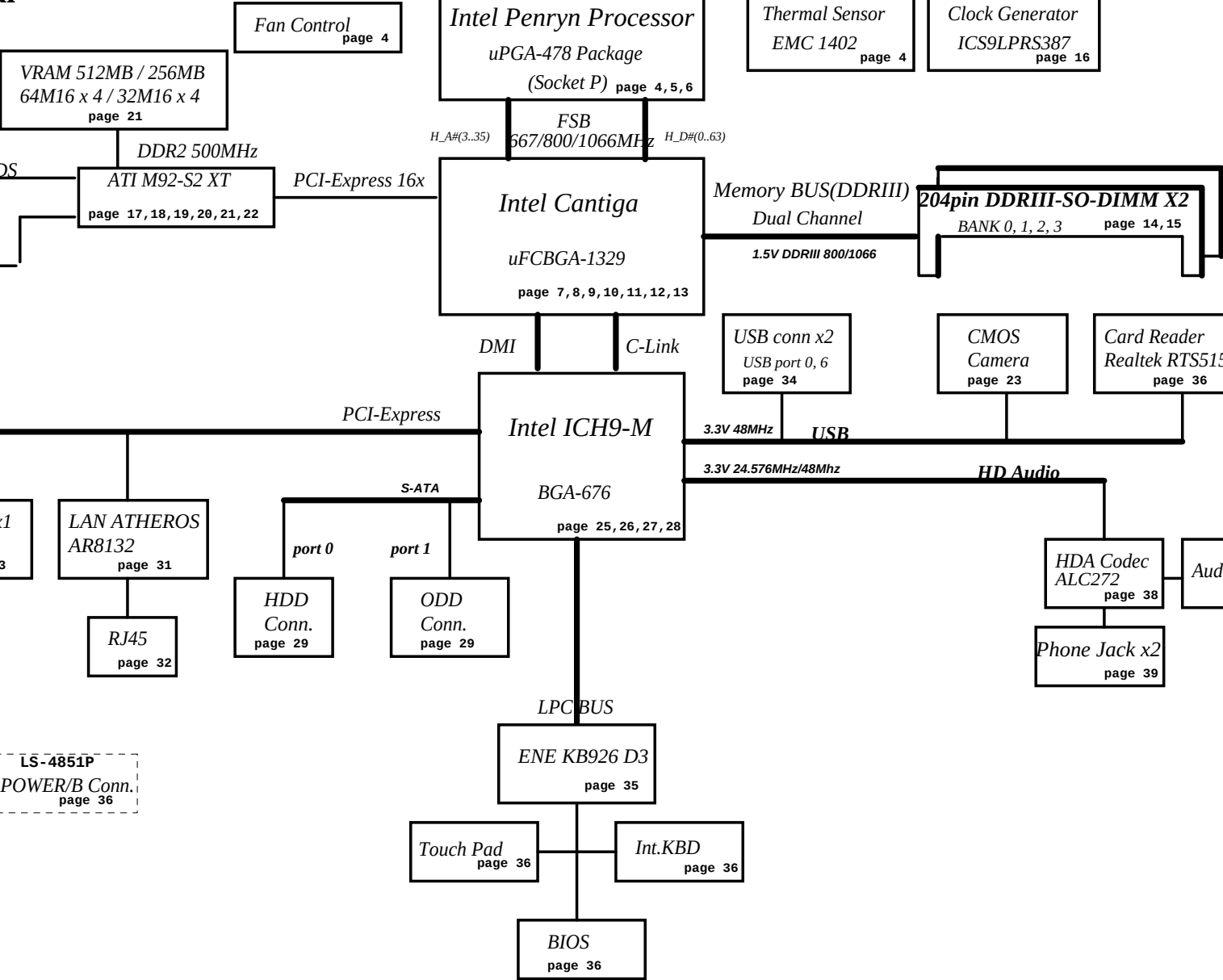
2009-09-17

REV:1.0

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Model Name : NAWF2
File Name : LA-4853P
P/N : DA60000FI00
P/N : DA60000FI10



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for GMCH LVDS	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC 1402-1	1001 100X b
EEPROM(24C16/02)	1010 000X b	GMT G781-1	1001 101X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1(PVT2)
2	1.0(Pre-MP)
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45	GM@
8132	8132@

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

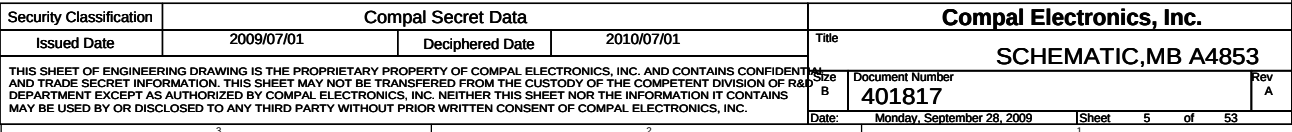
SATA table

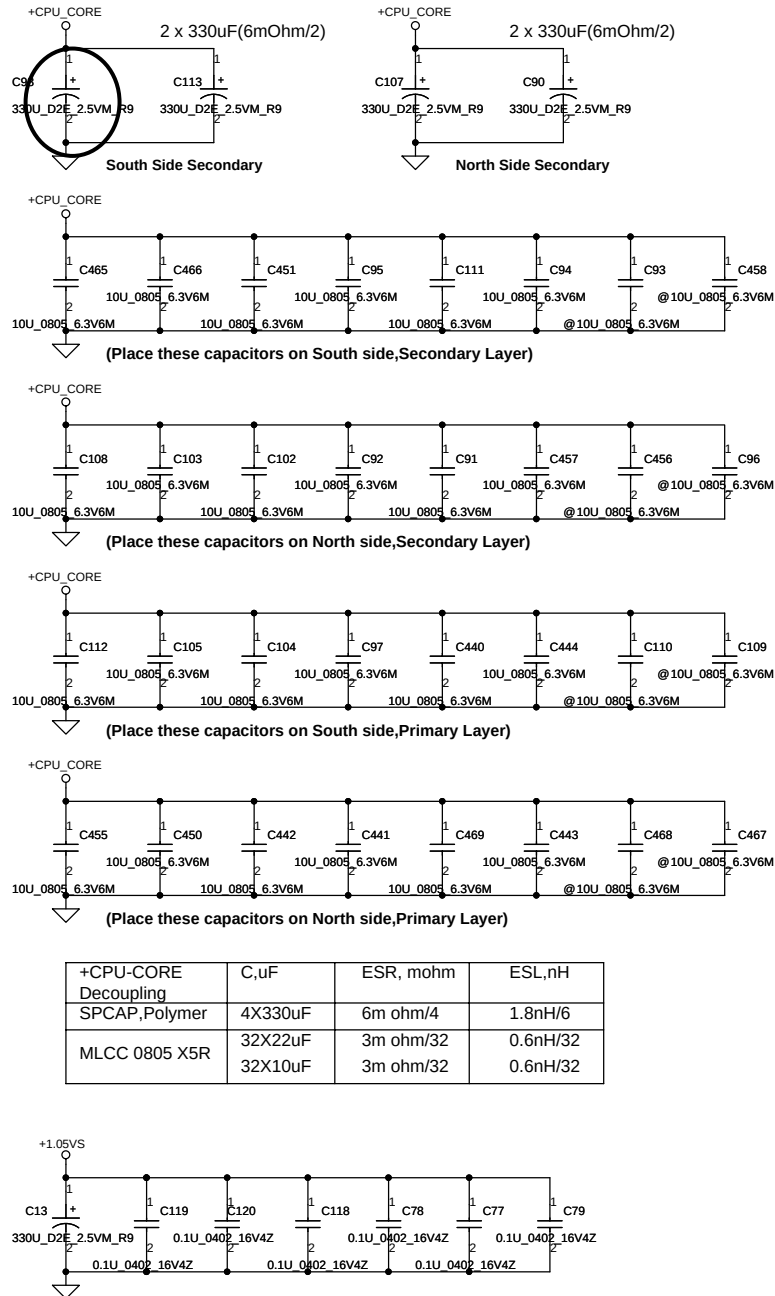
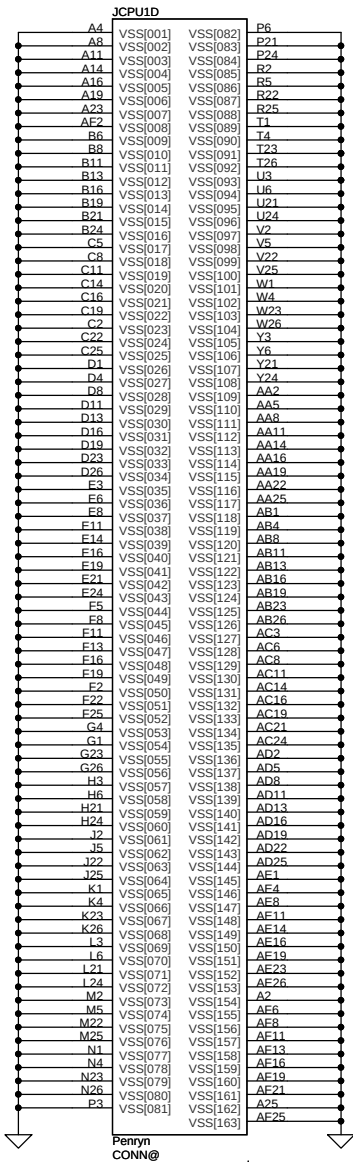
SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

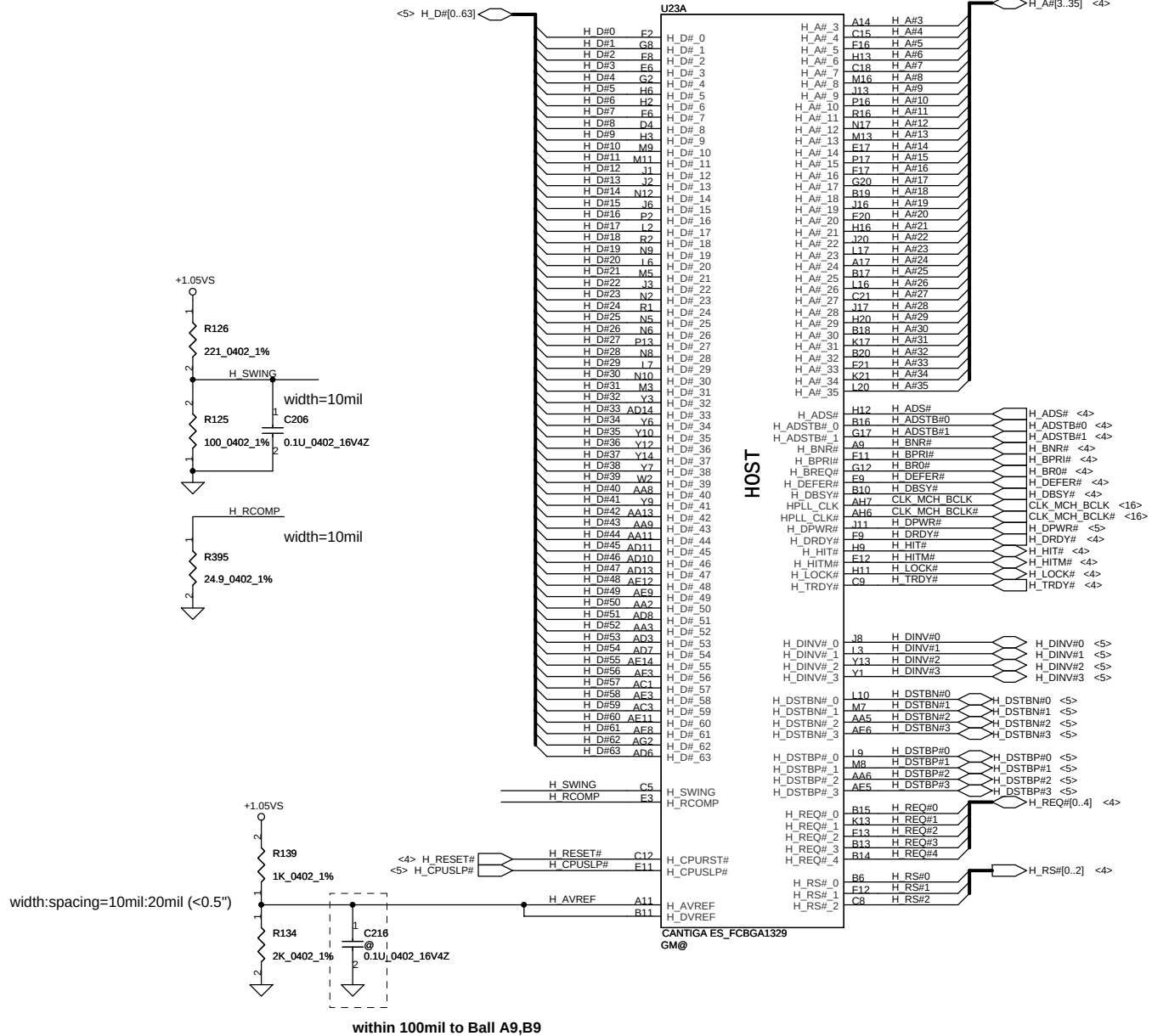
USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	
	UHCI2	Port2	
		Port3	CMOS Camera
EHCI2	UHCI3	Port4	Card Reader
		Port5	
	UHCI4	Port6	MB USB Conn.
		Port7	
EHCI2	UHCI5	Port8	
		Port9	
	UHCI6	Port10	Wireless Card
		Port11	

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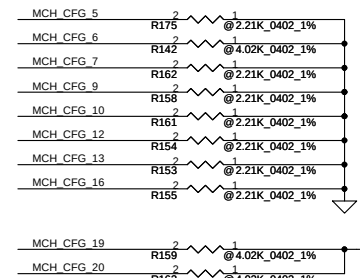


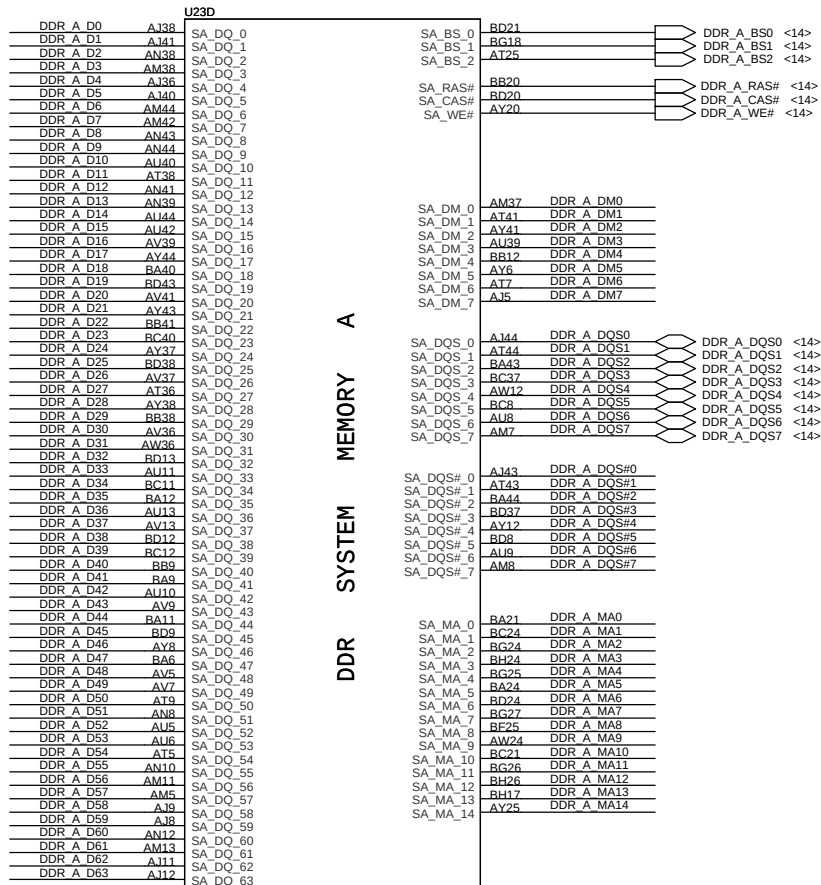
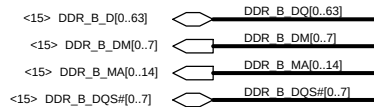
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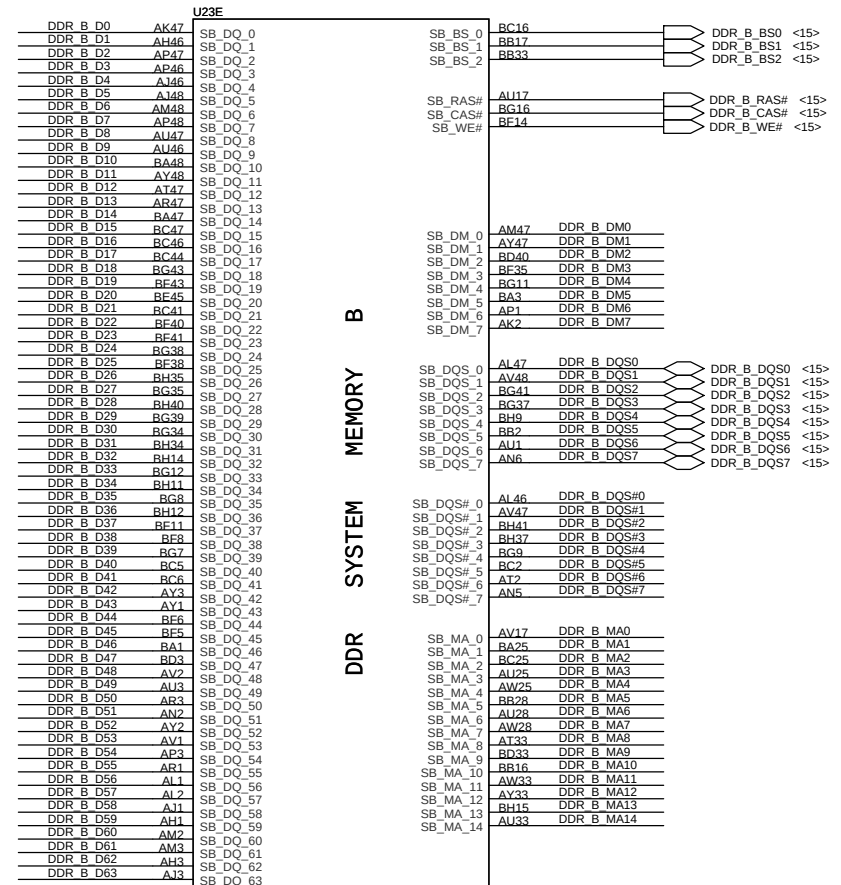
as close as possible to the related balls

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present



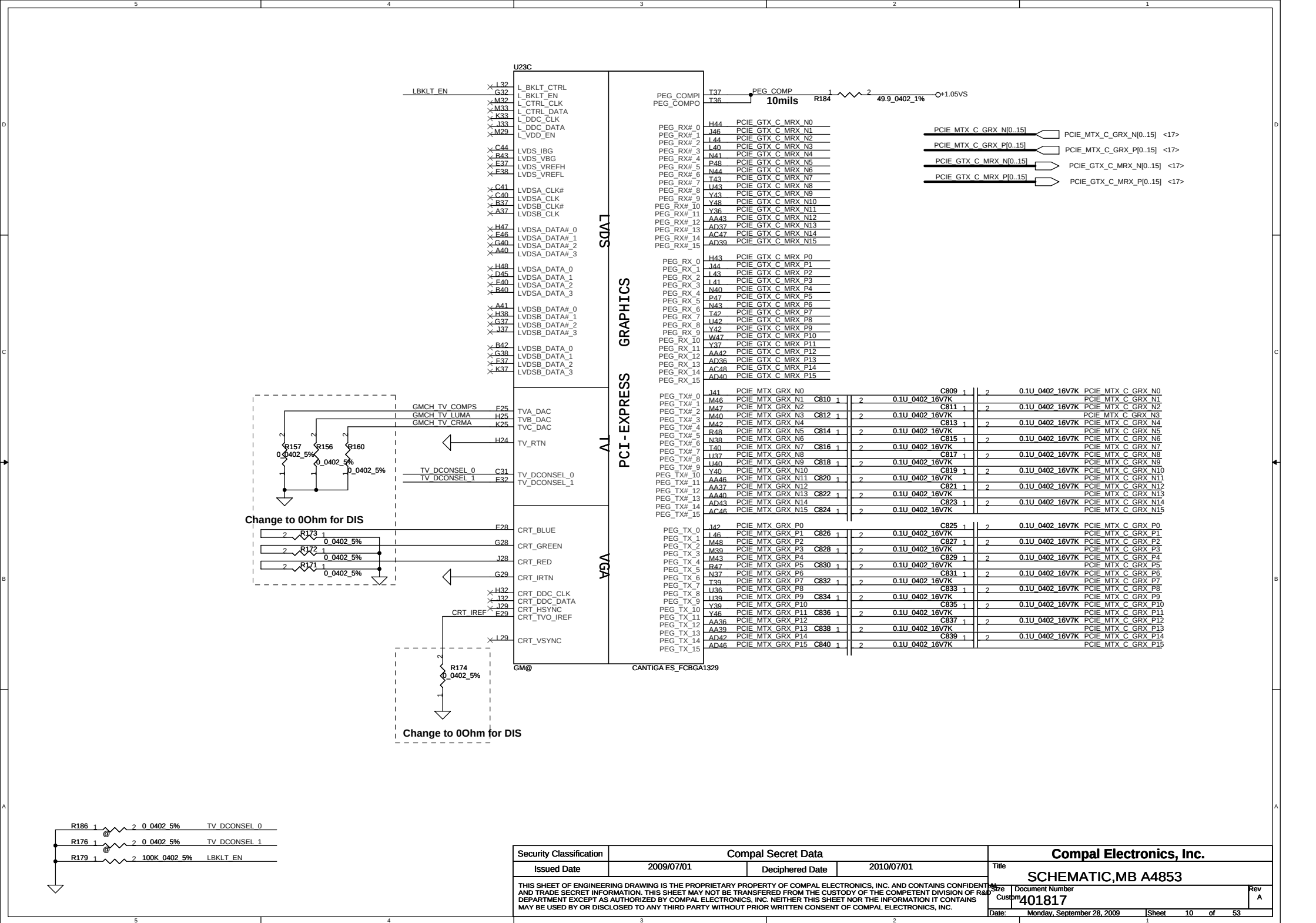


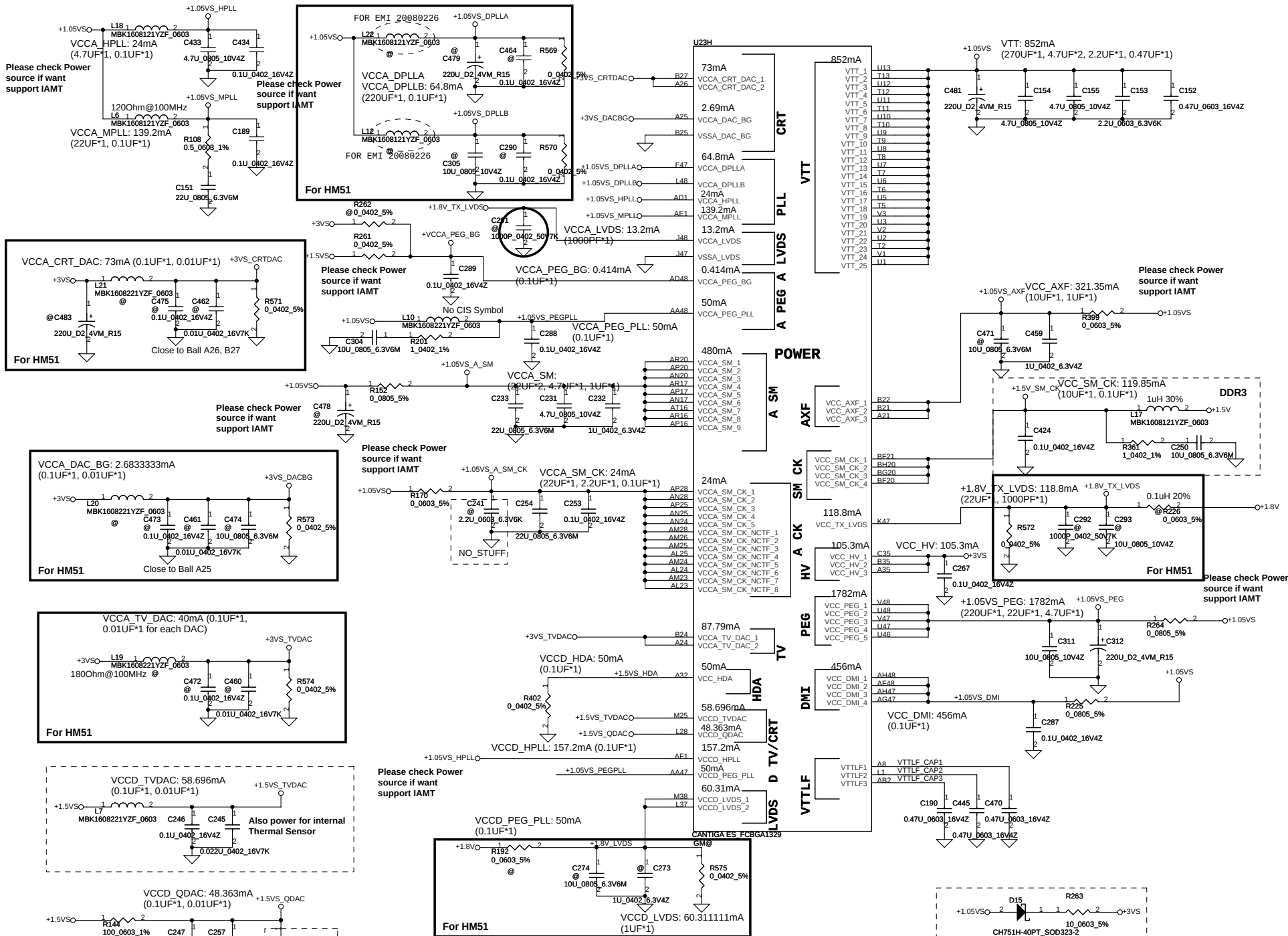
GM@ CANTIGA ES_FCBGA1329



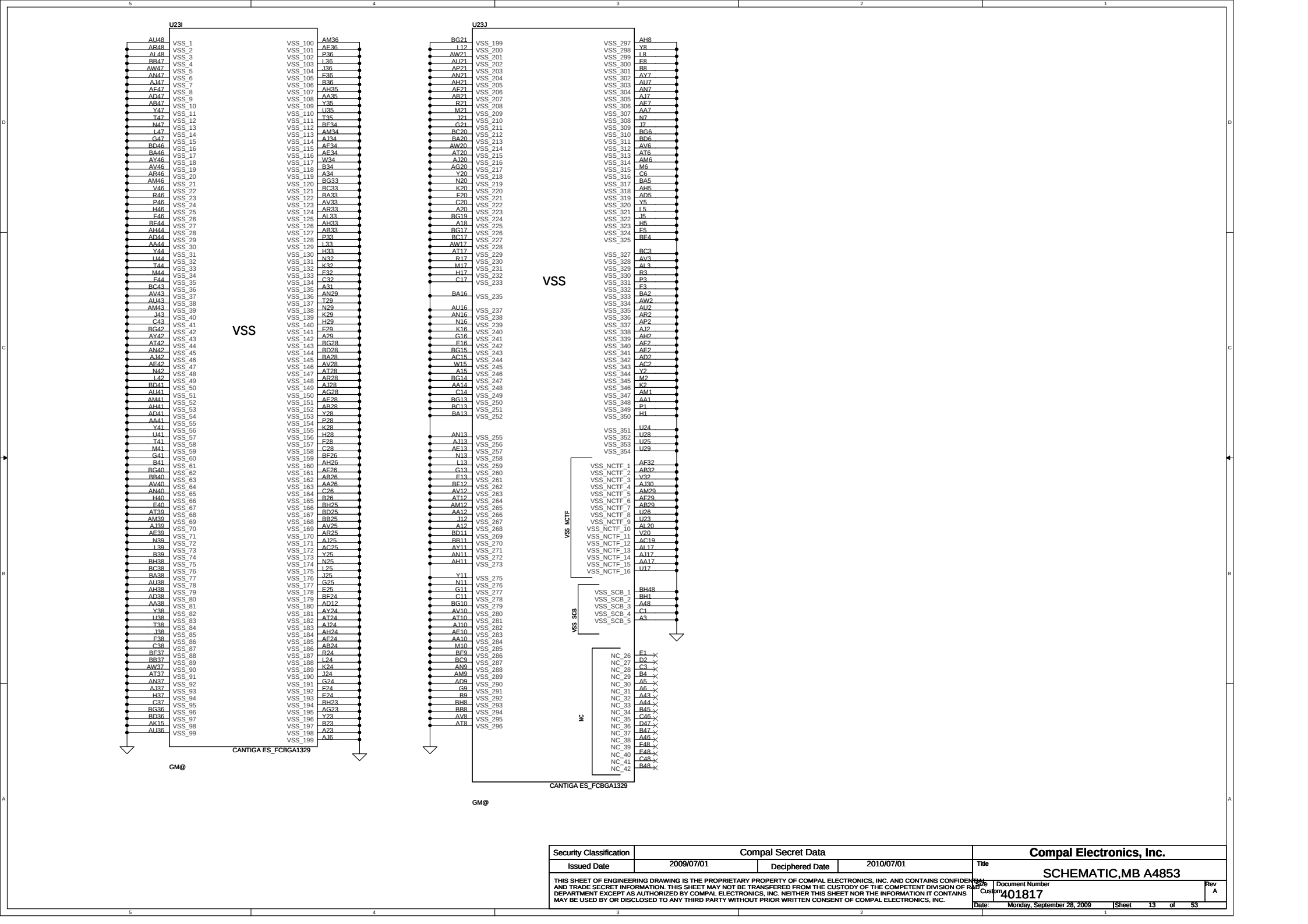
GM@ CANTIGA ES_FCBGA1329

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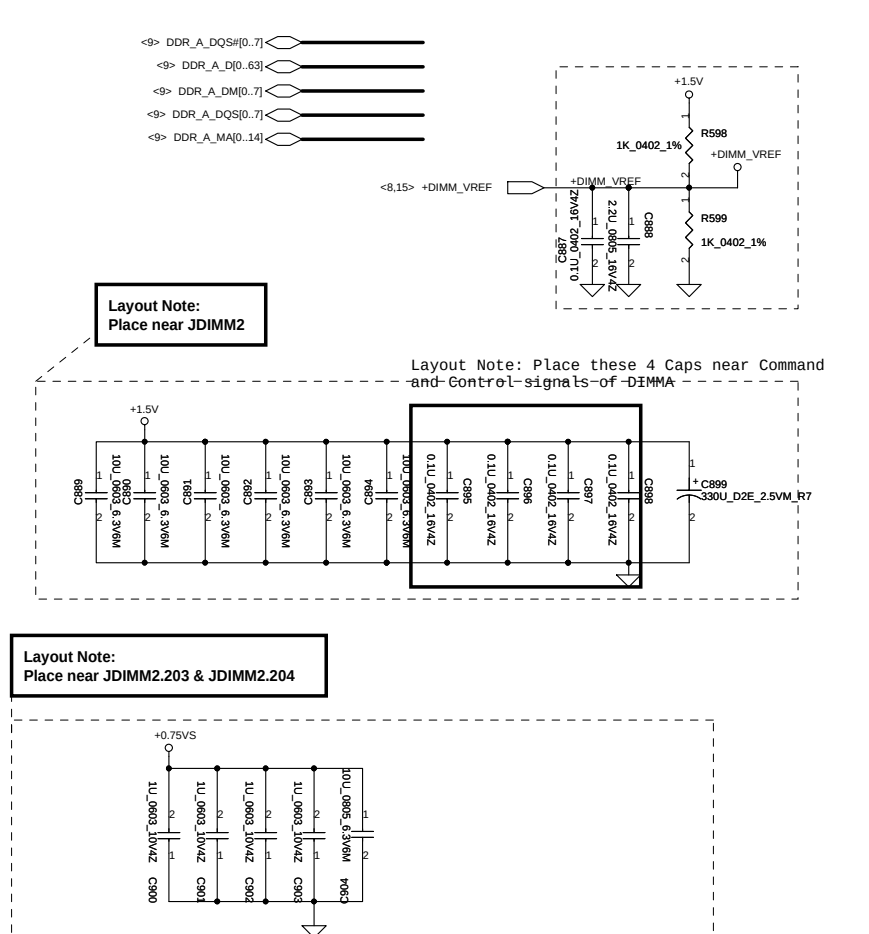
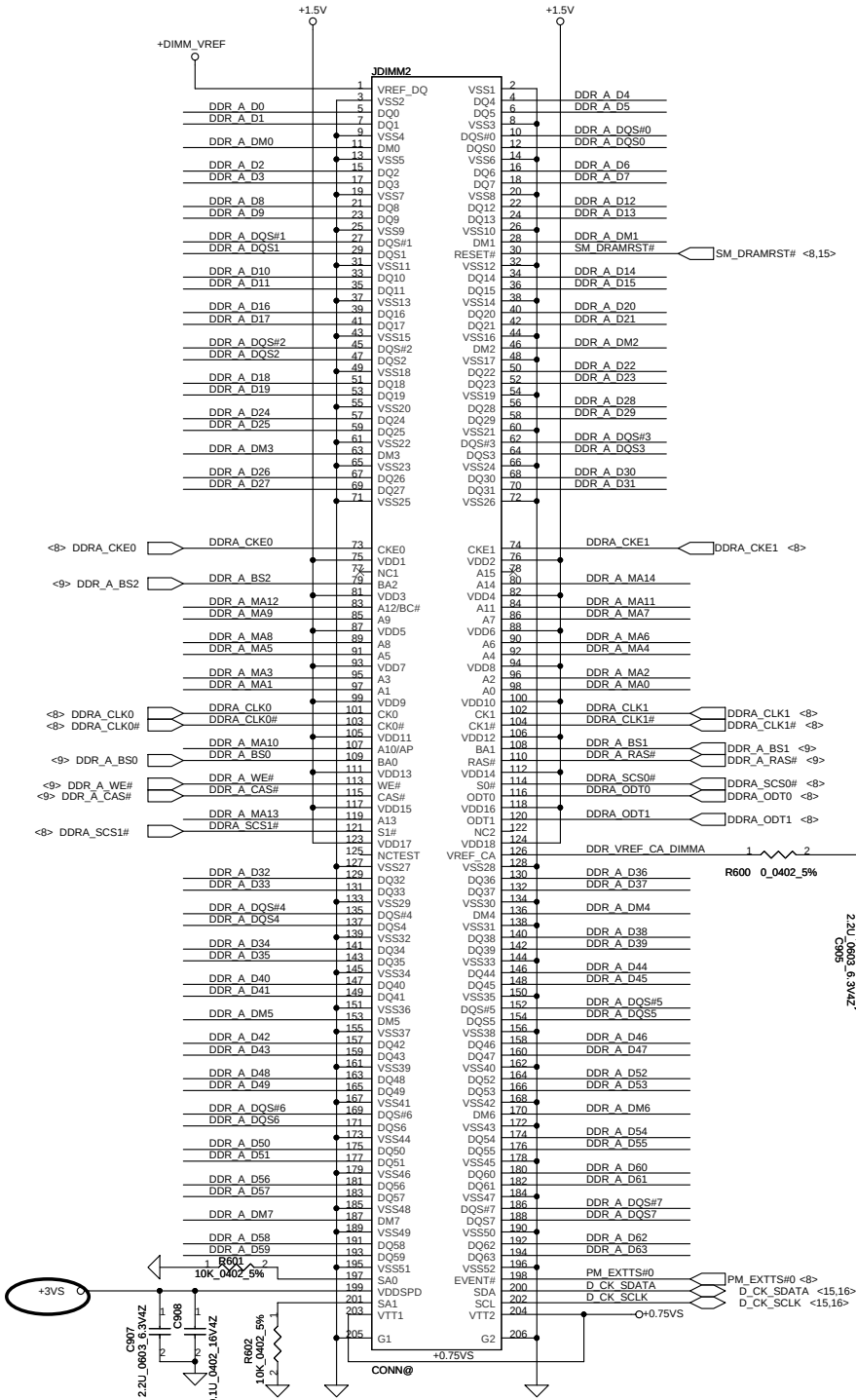


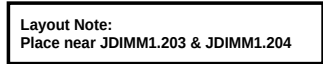
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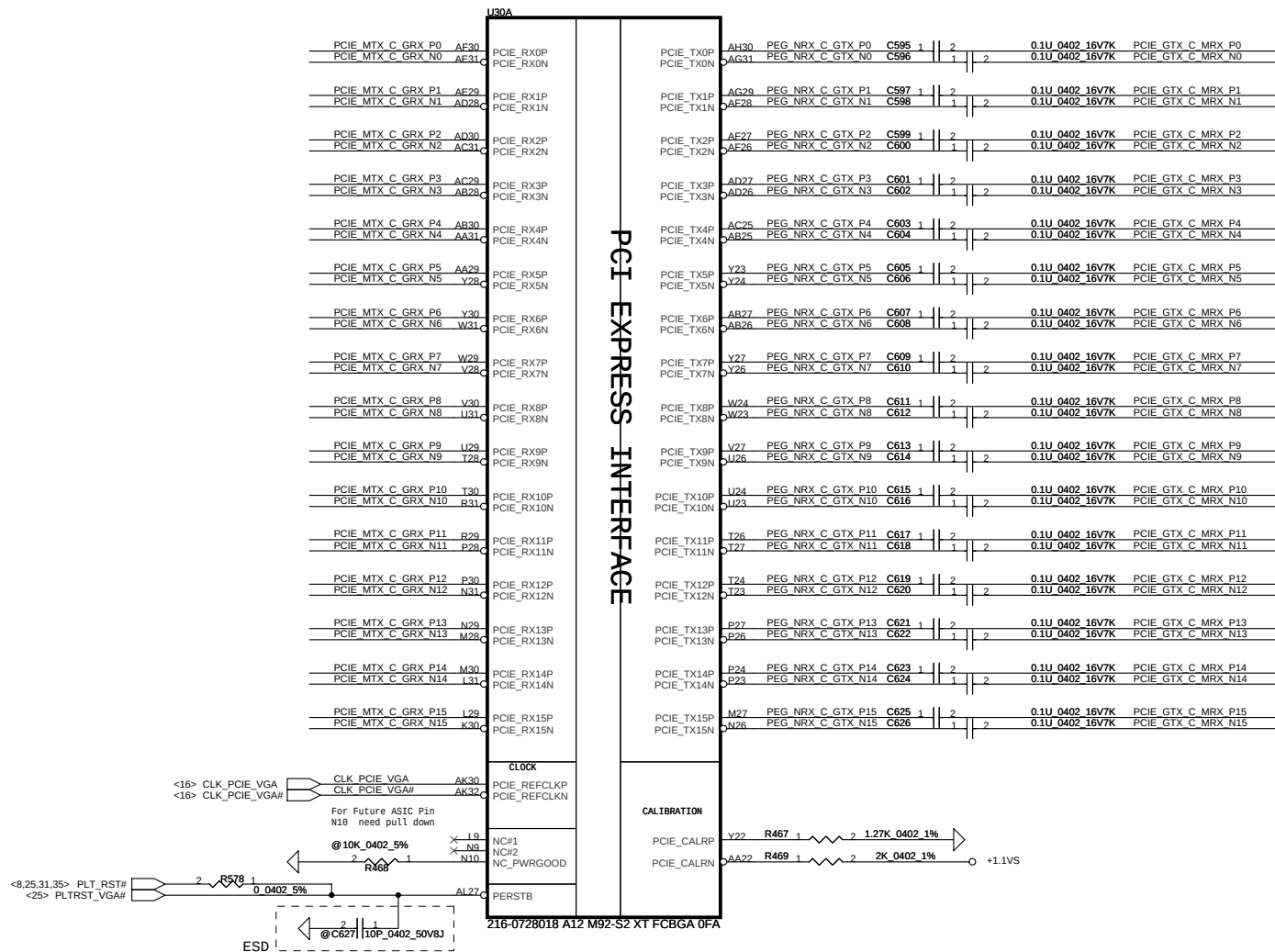
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
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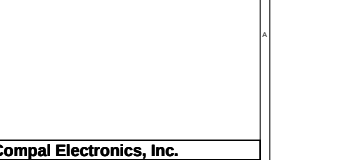
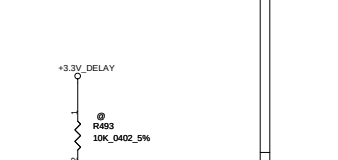
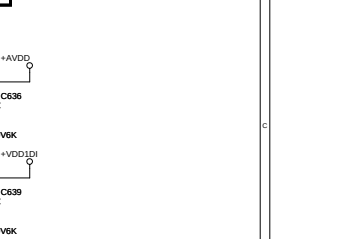
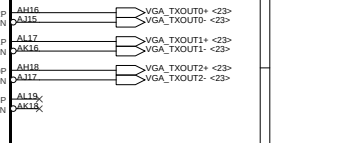
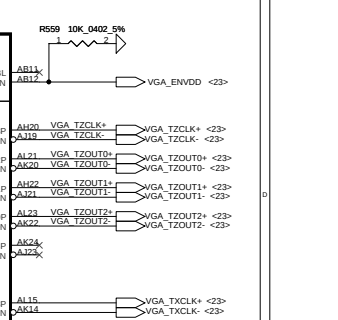
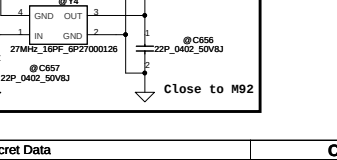
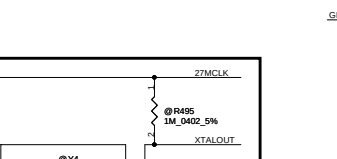
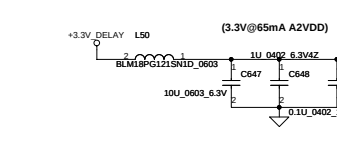
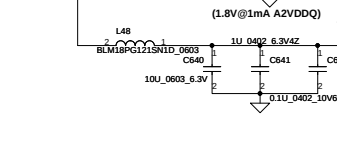
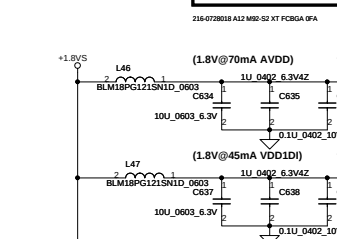
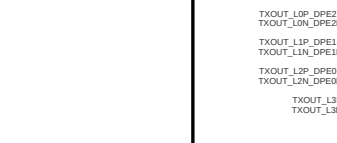
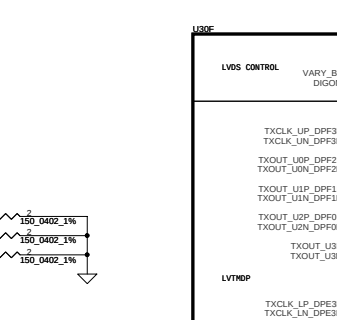
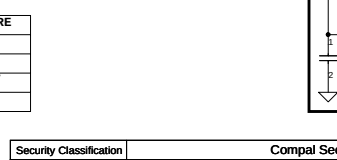
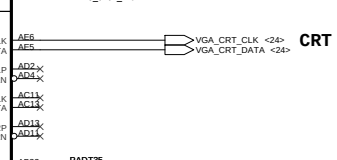
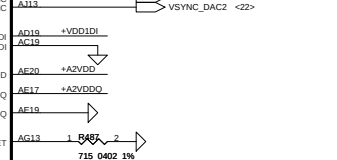
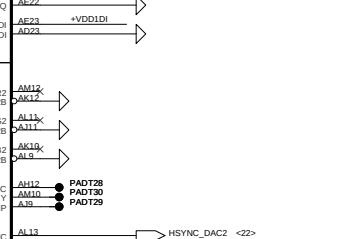
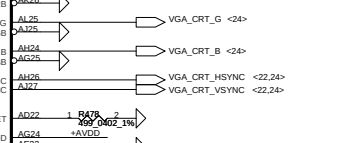
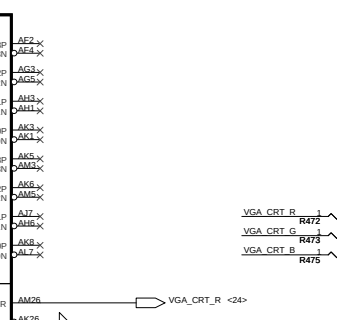
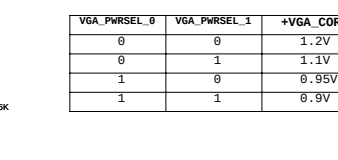
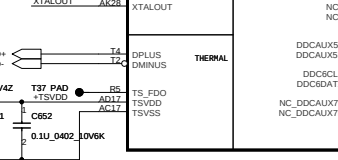
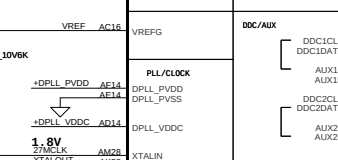
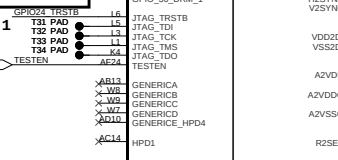
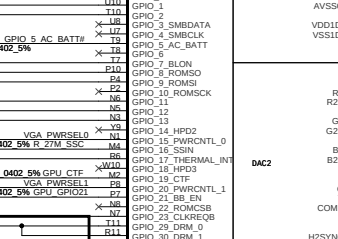
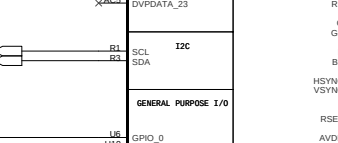
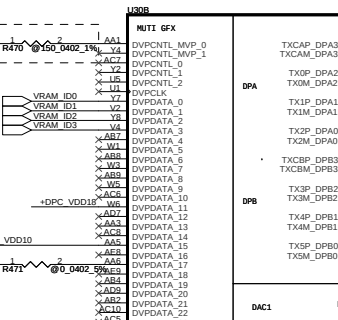
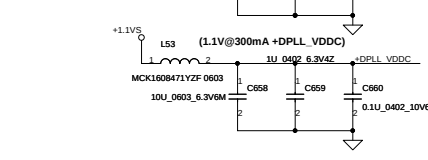
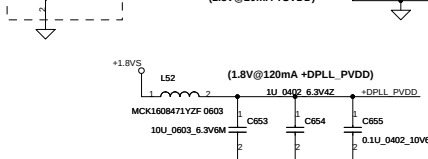
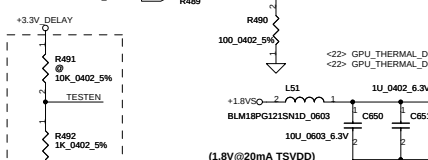
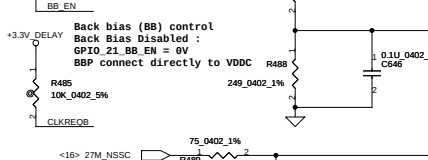
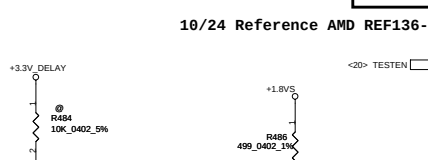
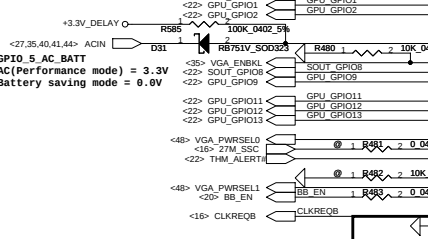
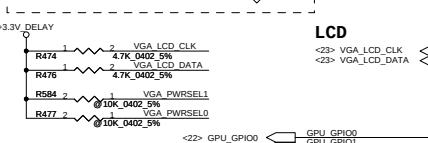
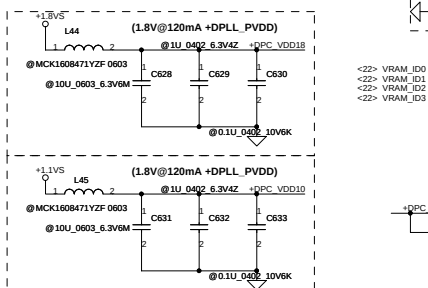
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<10> PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]
<10> PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX P[0..15]
<10> PCIE_MTX_C_GRX_N[0..15] PCIE MTX C GRX N[0..15]

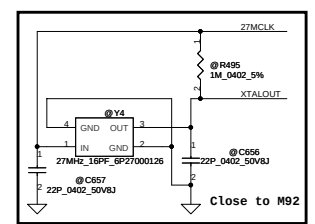


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For M92-S2: DO NOT Install any Component in this Box.

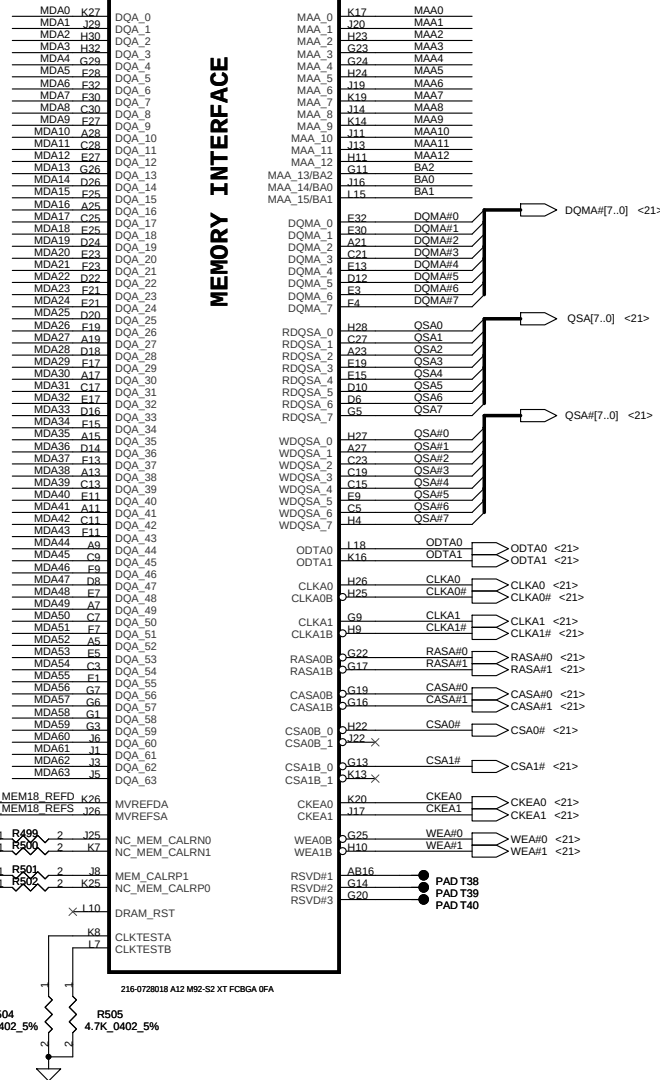


VGA_PwrSEL_0	VGA_PwrSEL_1	+VGA_CORE
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

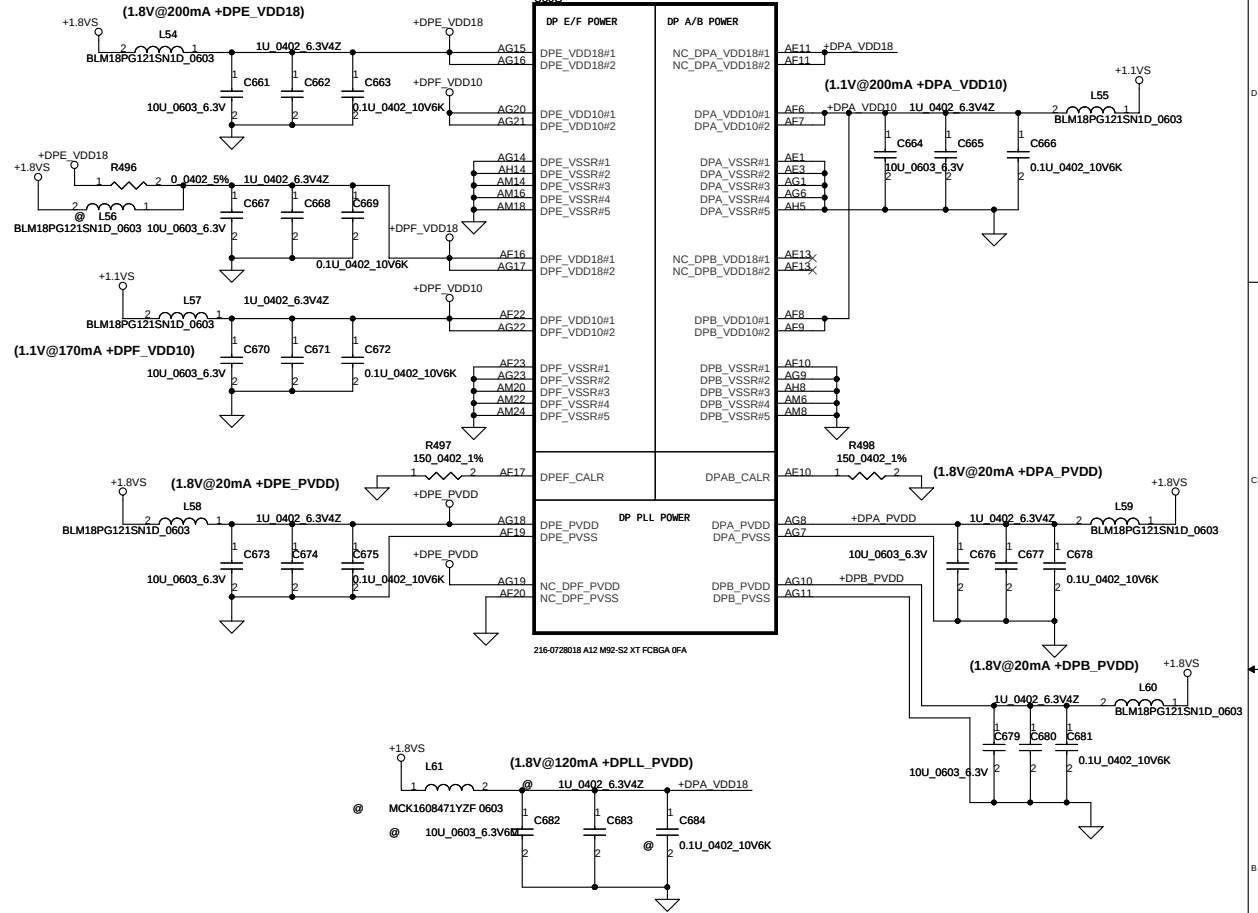


MAA[12..0] → MAA[12..0] <21>
 BAA[2..0] → BAA[2..0] <21>
 <21> MDA[63..0] ↔ MDA[63..0]

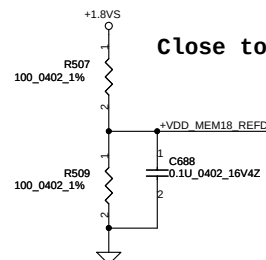
U30C



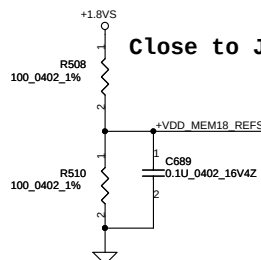
U30G



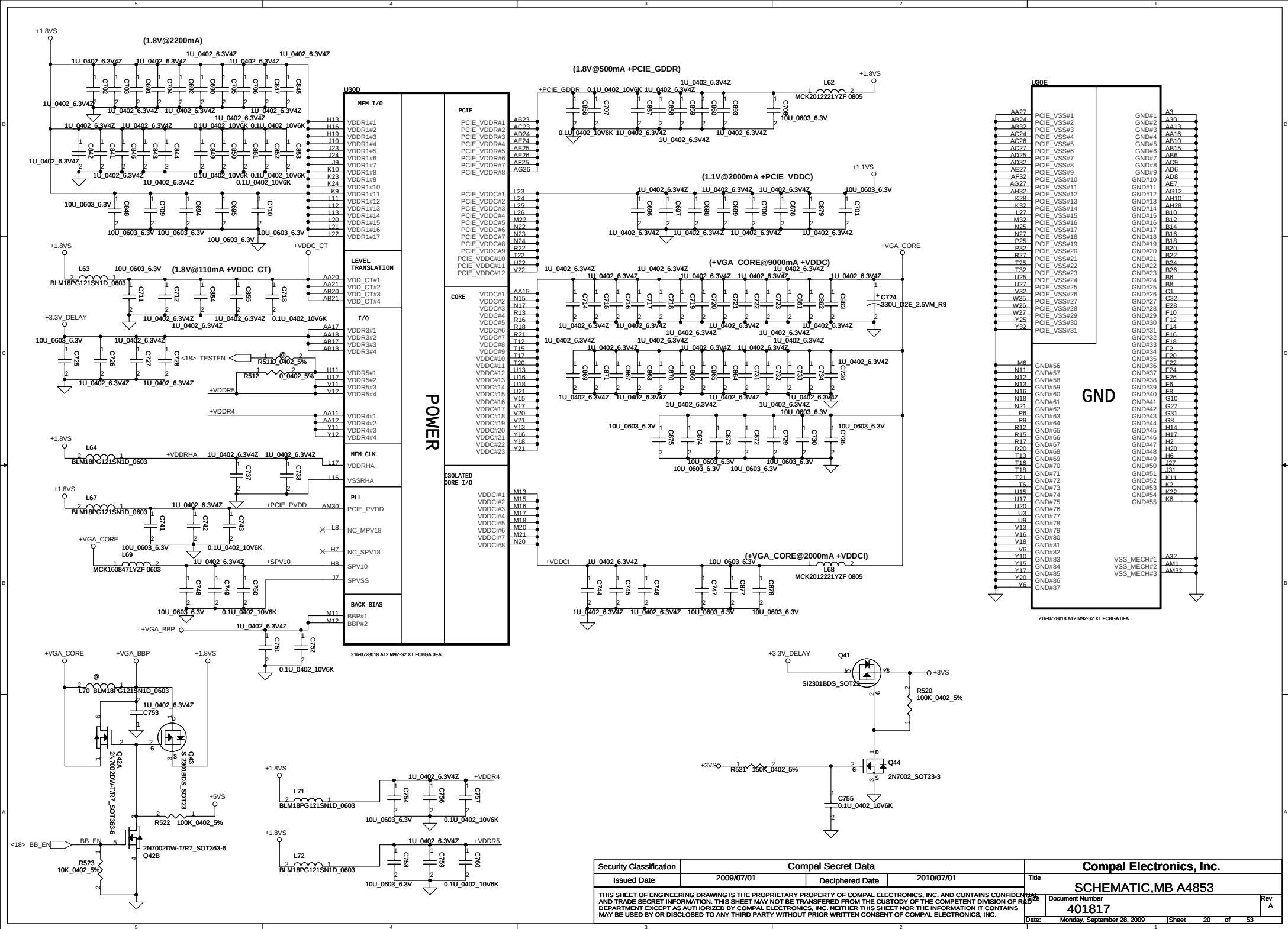
close to K26

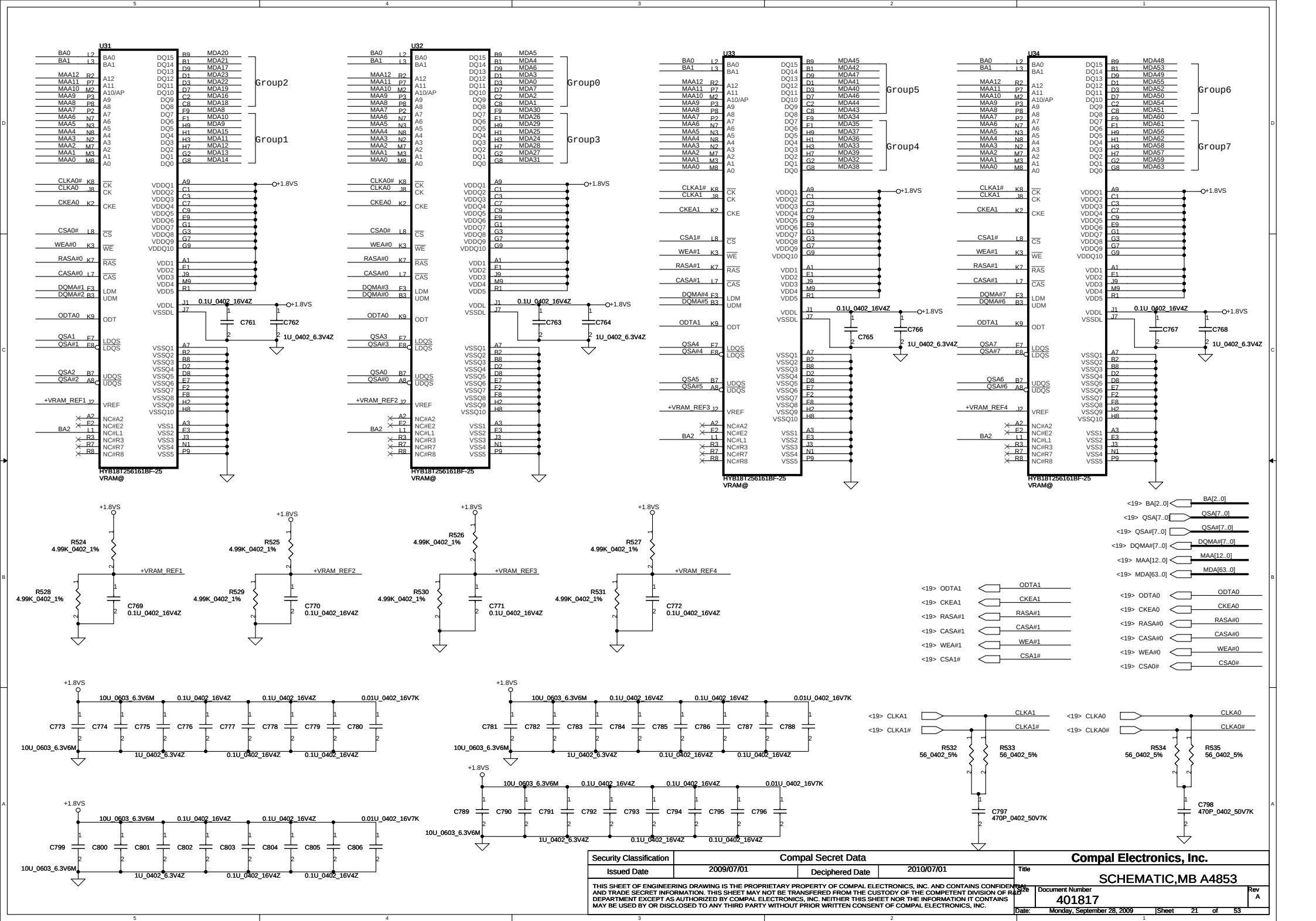


close to J26

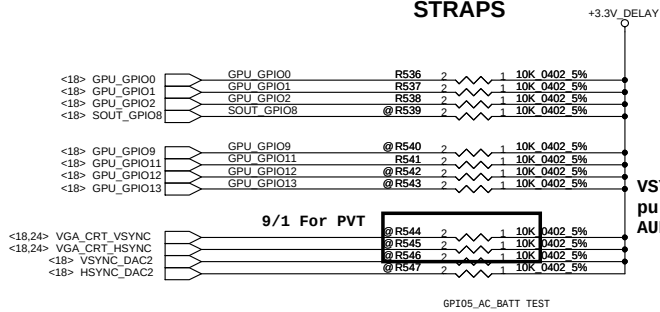


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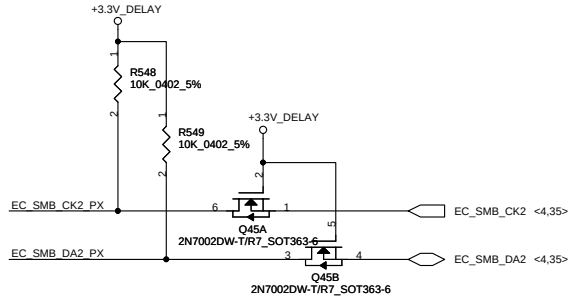




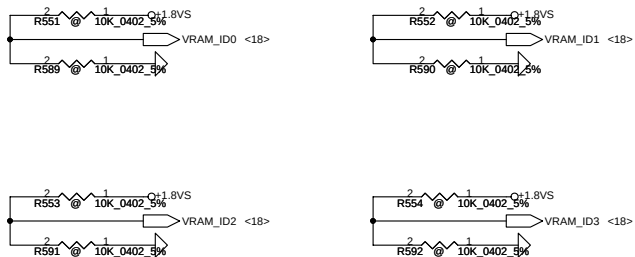
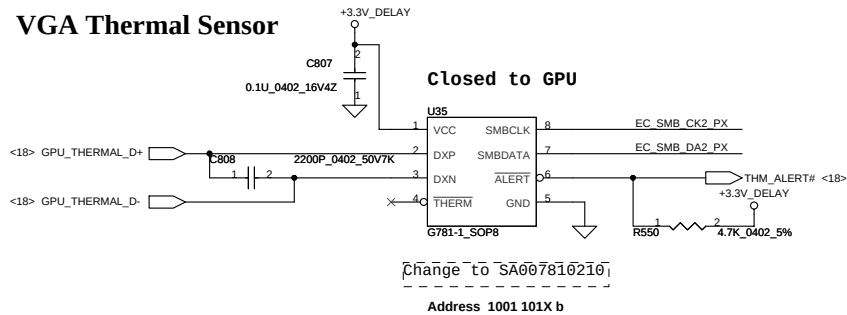
STRAPS



VSYNC_DAC1 and HSYNC_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO function



VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X
AUD[0]	VSYNC		

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

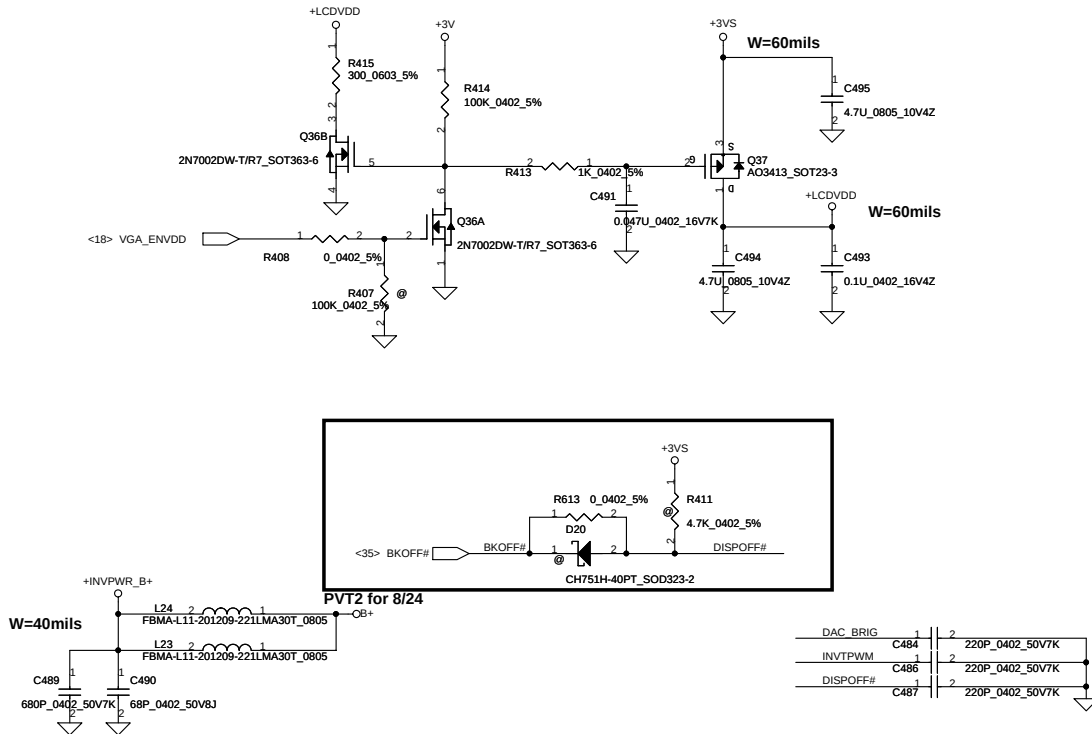
GPIO_28_TDO GPIO21_BB_EN

VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3

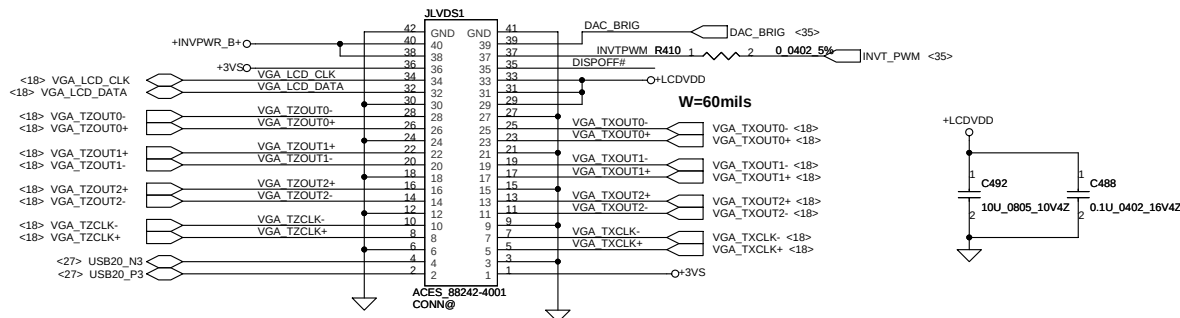
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-XT		256MB(x4)	Hynix 32Mx16 1.8V	SA00002DL10	1 0 0 0
				512MB(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
				512MB(x4)	ATI 64Mx16 1.8V	SA00003LT10	0 0 1 0
				512MB(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

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LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



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				Rev	A

CRT Connector

W=40mils

3V3_VCC

1.1A_6VDC_FUSE

C12 0.1U_0402_16V4Z

D4 RB491D_SC59-3

F1

D26 DAN217_SC59

D25 DAN217_SC59

+3V3_VCC

C560 8P_0402_50V8J

C559 8P_0402_50V8J

C558 8P_0402_50V8J

C57 100P_0402_50V8J

C89 10P_0402_50V8J

C76 10P_0402_50V8J

C101 68P_0402_50V8J

C62 68P_0402_50V8J

C547 3.3P_0402_50V8J

C534 3.3P_0402_50V8J

C532 3.3P_0402_50V8J

C546 8P_0402_50V8J

C535 8P_0402_50V8J

C533 8P_0402_50V8J

L42 FCM2012C-800_0805

L41 FCM2012C-800_0805

L40 FCM2012C-800_0805

L39 FCM2012C-800_0805

L31 FCM2012C-800_0805

L30 FCM2012C-800_0805

L4 0.0603_5%

L3 0.0603_5%

R464 150_0402_1%

R443 150_0402_1%

R442 150_0402_1%

R40 10K_0402_5%

R463 100K_0402_5%

R50 2.2K_0402_5%

R29 2.2K_0402_5%

R581 10K_0402_5%

R582 10K_0402_5%

U4 74AHCT1G125GW_SOT353-5

U3 74AHCT1G125GW_SOT353-5

U6 2N7002_SOT23

Q4 2N7002_SOT23

CRT_R_1

CRT_G_1

CRT_B_1

CRT_HSYNC_1

CRT_VSYNC_1

CRT_R_2

CRT_G_2

CRT_B_2

CRT_HSYNC_2

CRT_VSYNC_2

DDCCLK

DDCDATA

VGA_CRT_R

VGA_CRT_G

VGA_CRT_B

VGA_CRT_HSYNC

VGA_CRT_VSYNC

VGA_CRT_DATA

VGA_CRT_CLK

Change 3.3p For M92

Change 8p For M92

For HM51

For HM51

For HM51

Place closed to the chipset

+3.3V_DELAY

3V3_VCC

1.1A_6VDC_FUSE

C12 0.1U_0402_16V4Z

D4 RB491D_SC59-3

F1

D26 DAN217_SC59

D25 DAN217_SC59

+3V3_VCC

C560 8P_0402_50V8J

C559 8P_0402_50V8J

C558 8P_0402_50V8J

C57 100P_0402_50V8J

C89 10P_0402_50V8J

C76 10P_0402_50V8J

C101 68P_0402_50V8J

C62 68P_0402_50V8J

C547 3.3P_0402_50V8J

C534 3.3P_0402_50V8J

C532 3.3P_0402_50V8J

C546 8P_0402_50V8J

C535 8P_0402_50V8J

C533 8P_0402_50V8J

L42 FCM2012C-800_0805

L41 FCM2012C-800_0805

L40 FCM2012C-800_0805

L39 FCM2012C-800_0805

L31 FCM2012C-800_0805

L30 FCM2012C-800_0805

L4 0.0603_5%

L3 0.0603_5%

R464 150_0402_1%

R443 150_0402_1%

R442 150_0402_1%

R40 10K_0402_5%

R463 100K_0402_5%

R50 2.2K_0402_5%

R29 2.2K_0402_5%

R581 10K_0402_5%

R582 10K_0402_5%

U4 74AHCT1G125GW_SOT353-5

U3 74AHCT1G125GW_SOT353-5

U6 2N7002_SOT23

Q4 2N7002_SOT23

CRT_R_1

CRT_G_1

CRT_B_1

CRT_HSYNC_1

CRT_VSYNC_1

CRT_R_2

CRT_G_2

CRT_B_2

CRT_HSYNC_2

CRT_VSYNC_2

DDCCLK

DDCDATA

VGA_CRT_R

VGA_CRT_G

VGA_CRT_B

VGA_CRT_HSYNC

VGA_CRT_VSYNC

VGA_CRT_DATA

VGA_CRT_CLK

Change 3.3p For M92

Change 8p For M92

For HM51

For HM51

For HM51

Place closed to the chipset

+3.3V_DELAY

3V3_VCC

1.1A_6VDC_FUSE

C12 0.1U_0402_16V4Z

D4 RB491D_SC59-3

F1

D26 DAN217_SC59

D25 DAN217_SC59

+3V3_VCC

C560 8P_0402_50V8J

C559 8P_0402_50V8J

C558 8P_0402_50V8J

C57 100P_0402_50V8J

C89 10P_0402_50V8J

C76 10P_0402_50V8J

C101 68P_0402_50V8J

C62 68P_0402_50V8J

C547 3.3P_0402_50V8J

C534 3.3P_0402_50V8J

C532 3.3P_0402_50V8J

C546 8P_0402_50V8J

C535 8P_0402_50V8J

C533 8P_0402_50V8J

L42 FCM2012C-800_0805

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L31 FCM2012C-800_0805

L30 FCM2012C-800_0805

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R50 2.2K_0402_5%

R29 2.2K_0402_5%

R581 10K_0402_5%

R582 10K_0402_5%

U4 74AHCT1G125GW_SOT353-5

U3 74AHCT1G125GW_SOT353-5

U6 2N7002_SOT23

Q4 2N7002_SOT23

CRT_R_1

CRT_G_1

CRT_B_1

CRT_HSYNC_1

CRT_VSYNC_1

CRT_R_2

CRT_G_2

CRT_B_2

CRT_HSYNC_2

CRT_VSYNC_2

DDCCLK

DDCDATA

VGA_CRT_R

VGA_CRT_G

VGA_CRT_B

VGA_CRT_HSYNC

VGA_CRT_VSYNC

VGA_CRT_DATA

VGA_CRT_CLK

Change 3.3p For M92

Change 8p For M92

For HM51

For HM51

For HM51

Place closed to the chipset

+3.3V_DELAY

3V3_VCC

1.1A_6VDC_FUSE

C12 0.1U_0402_16V4Z

D4 RB491D_SC59-3

F1

D26 DAN217_SC59

D25 DAN217_SC59

+3V3_VCC

C560 8P_0402_50V8J

C559 8P_0402_50V8J

C558 8P_0402_50V8J

C57 100P_0402_50V8J

C89 10P_0402_50V8J

C76 10P_0402_50V8J

C101 68P_0402_50V8J

C62 68P_0402_50V8J

C547 3.3P_0402_50V8J

C534 3.3P_0402_50V8J

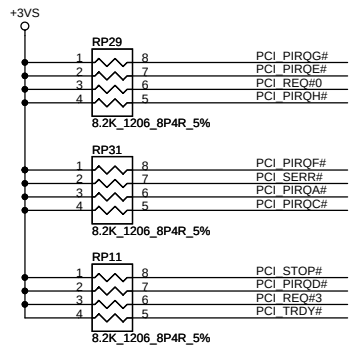
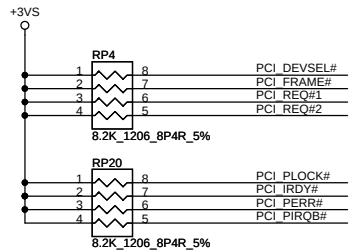
C532 3.3P_0402_50V8J

C546 8P_0402_50V8J

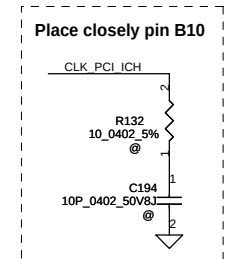
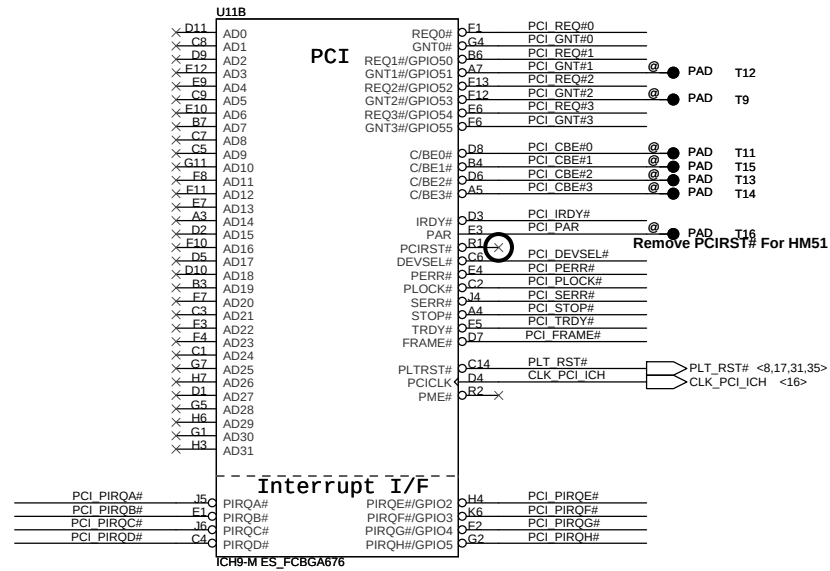
C535 8P_0402_50V8J

C533 8P_0402_50

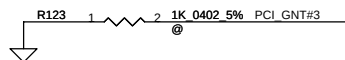
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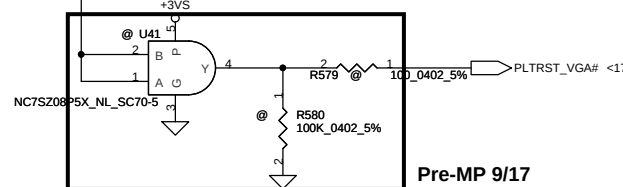
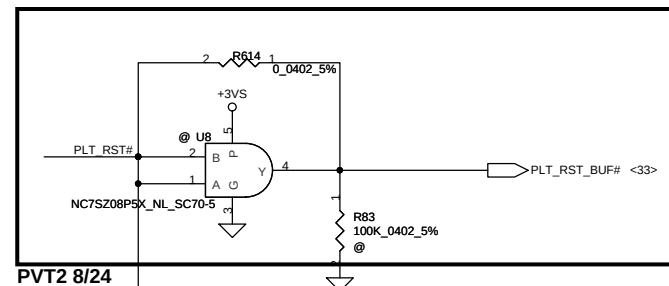
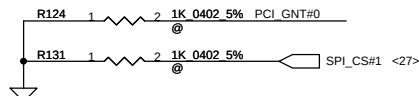
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



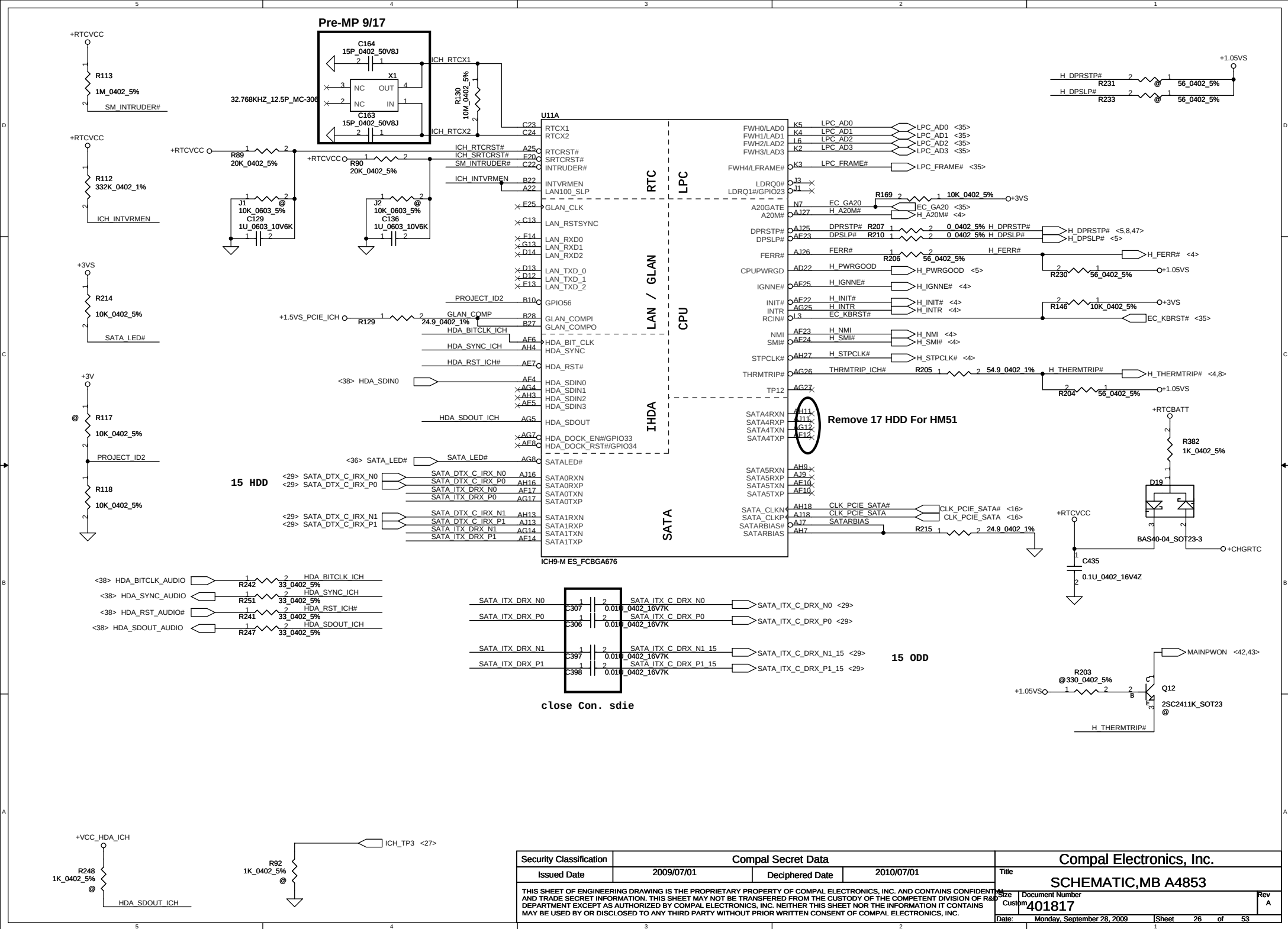
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

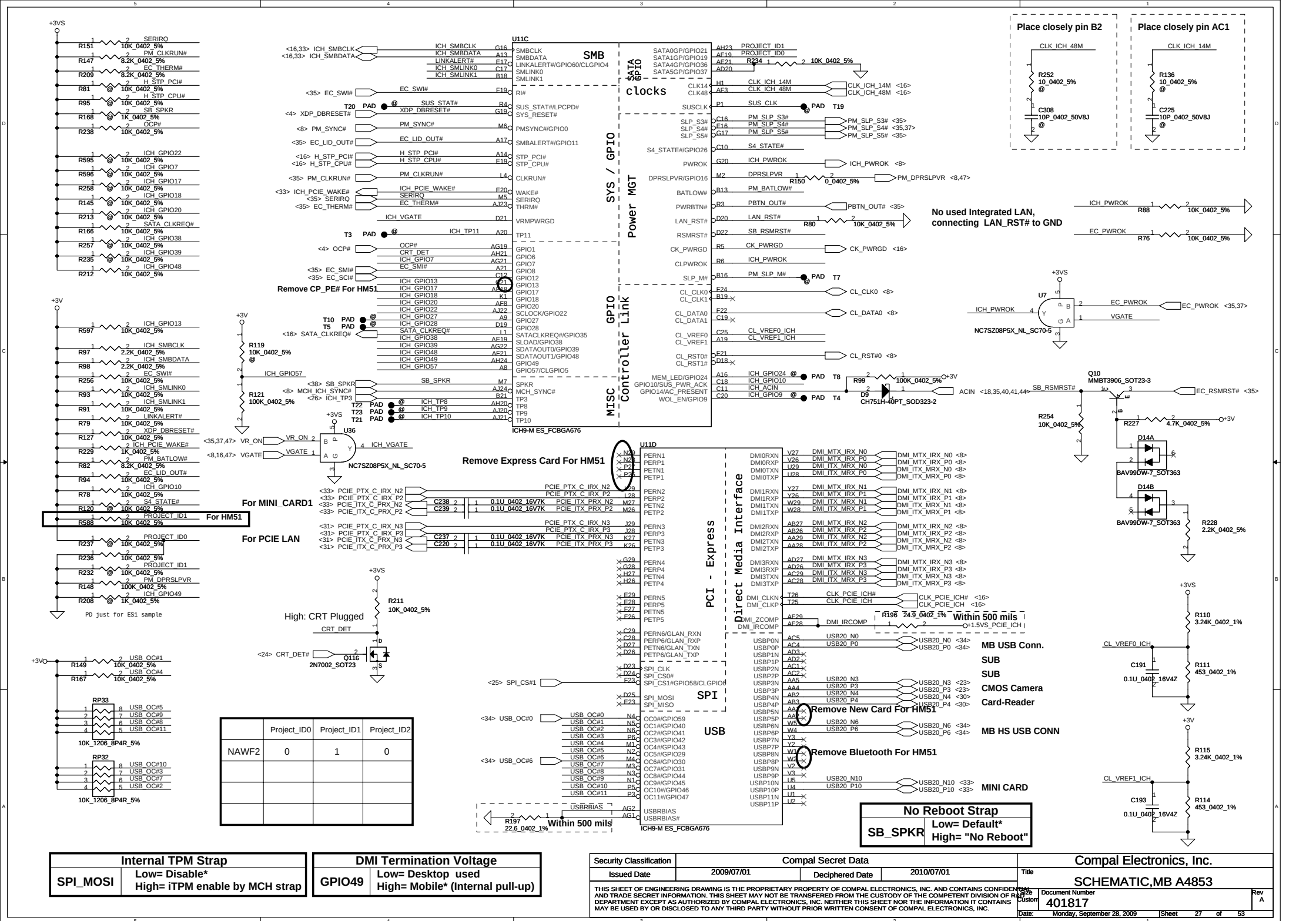


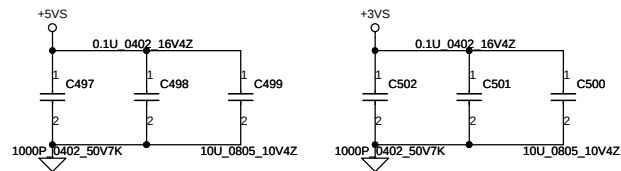
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



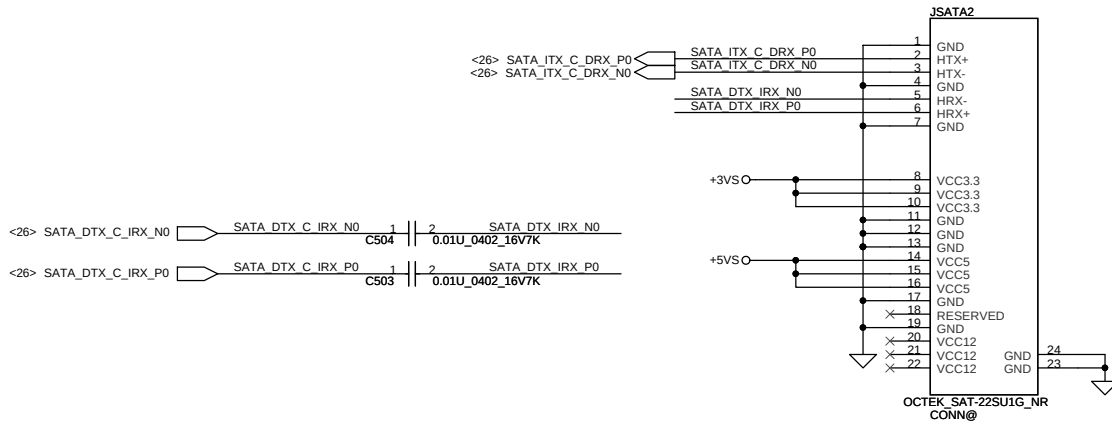
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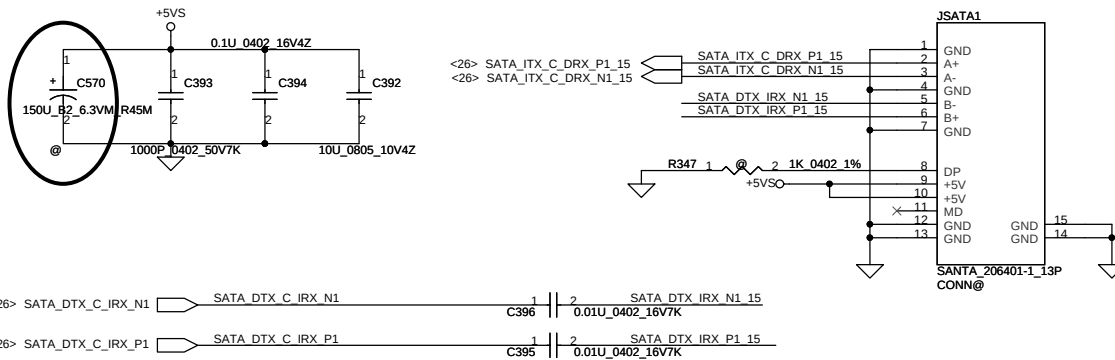




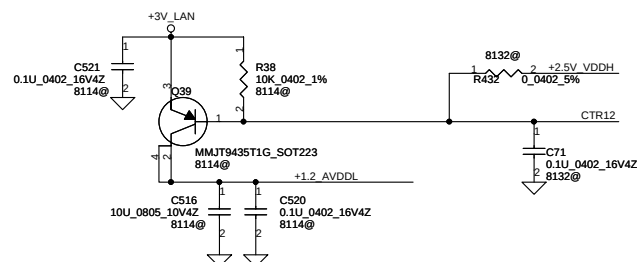
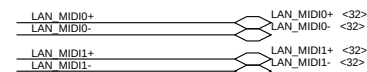
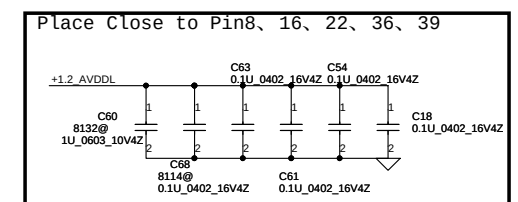
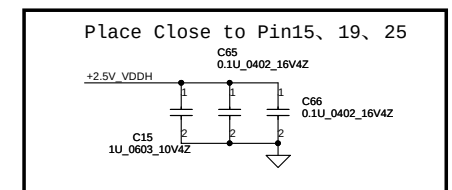
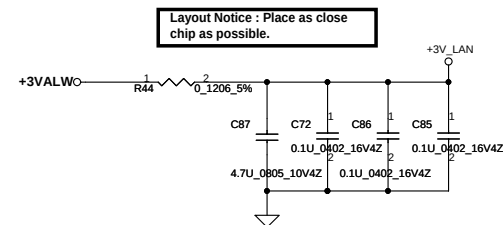
SATA HDD Conn.



SATA ODD Conn.

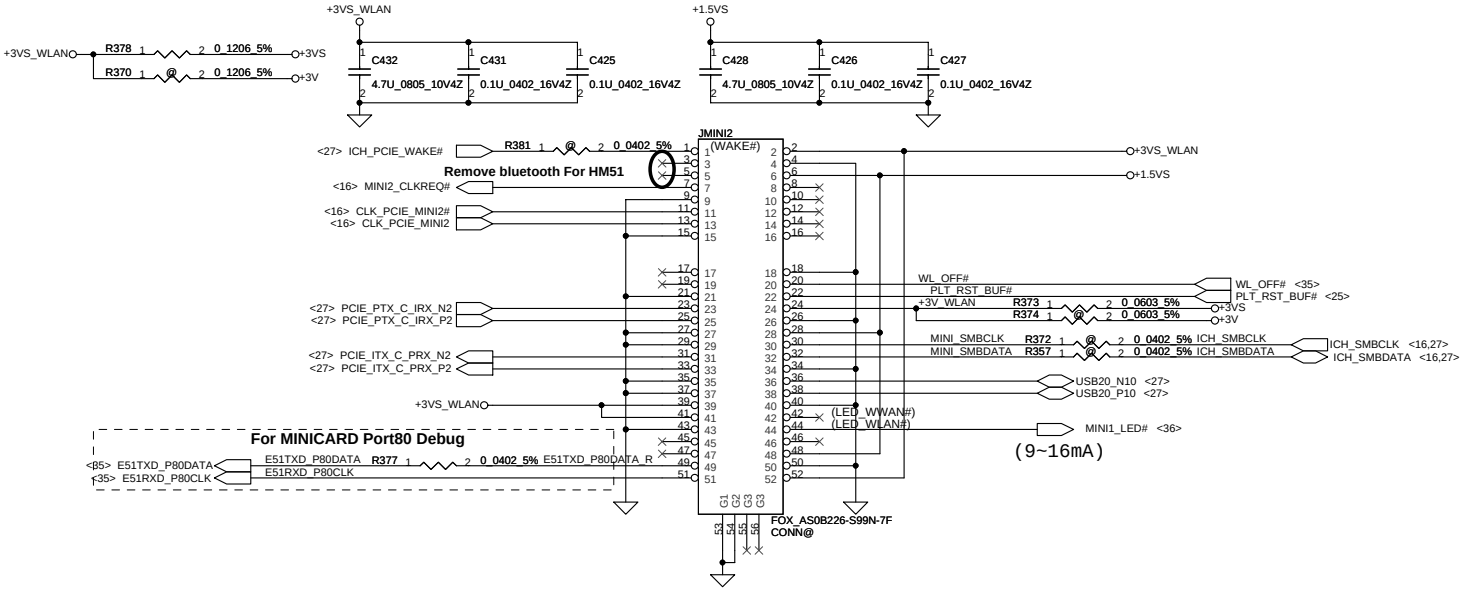


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				Sheet	29 of 53

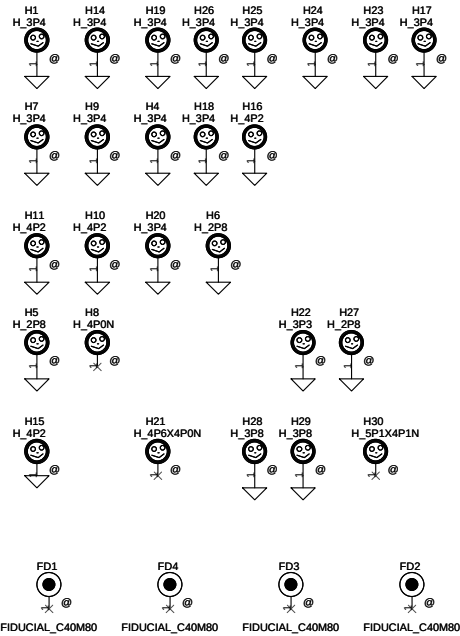


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						401817					
						Date:		Monday, September 28, 2009		Sheet 31 of 53	

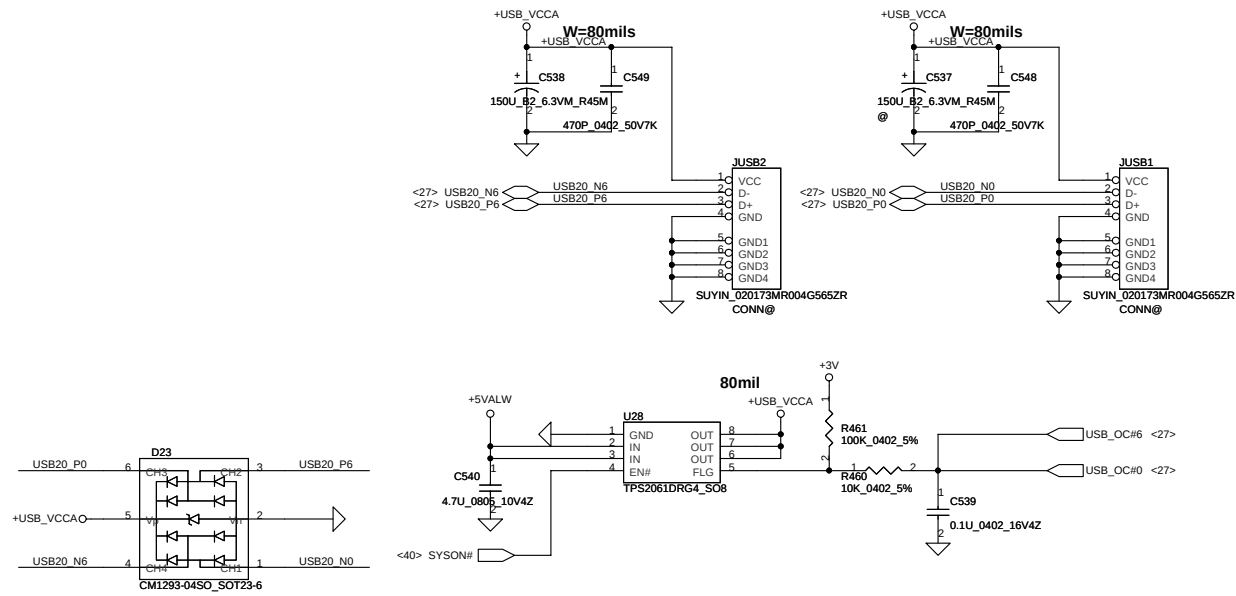
For Wireless LAN



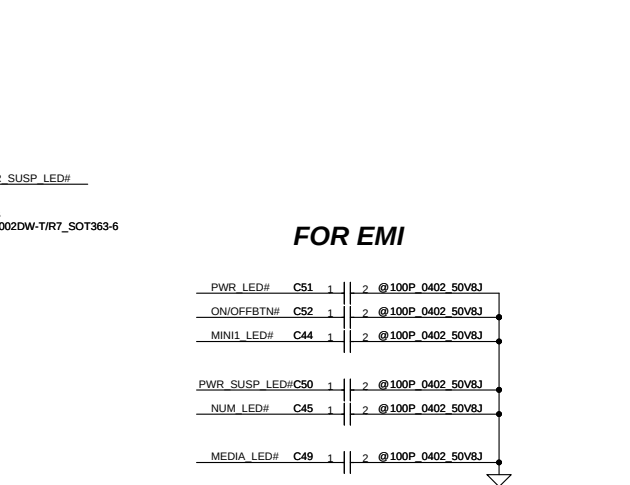
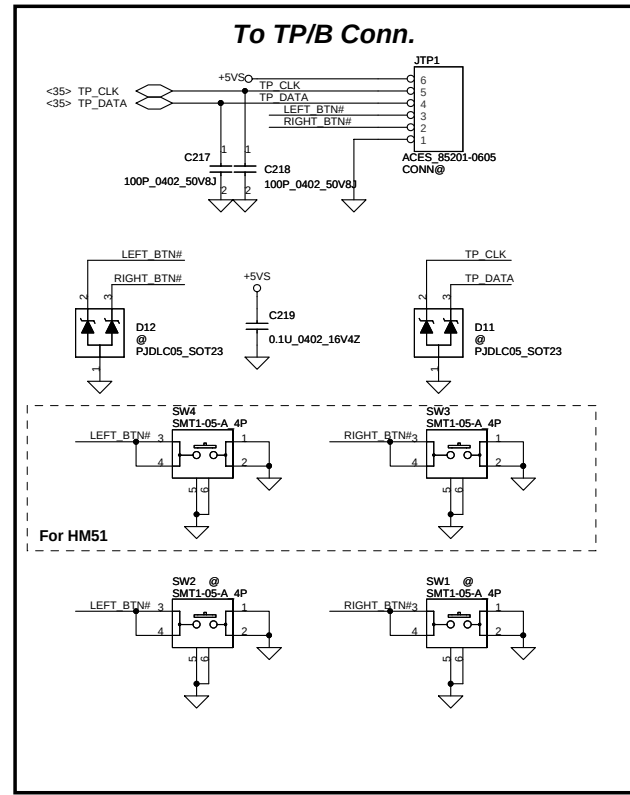
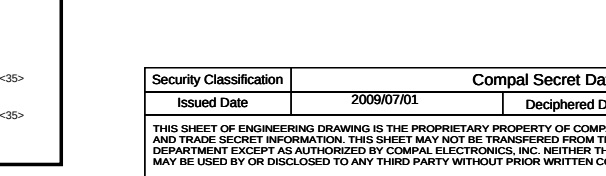
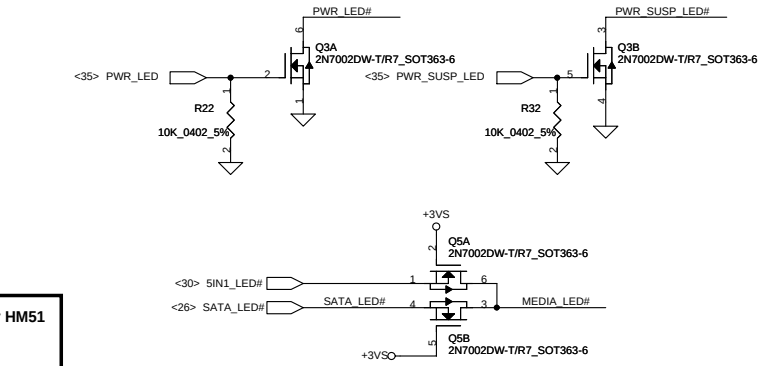
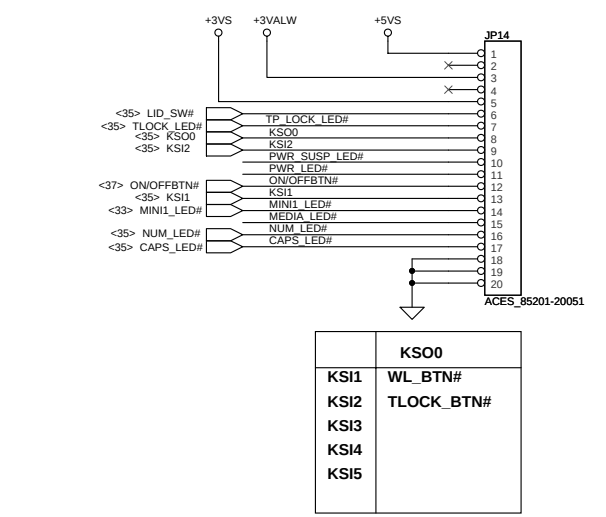
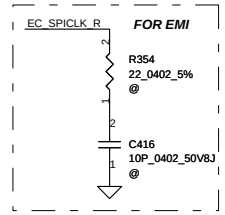
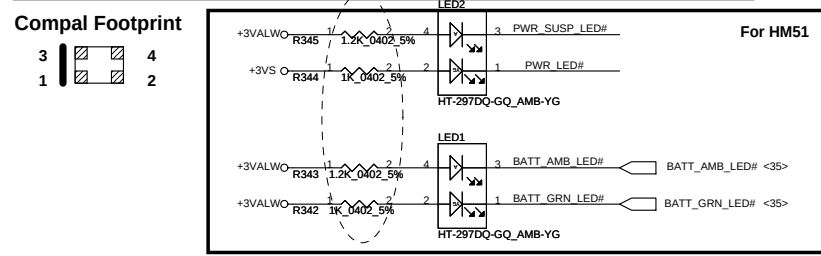
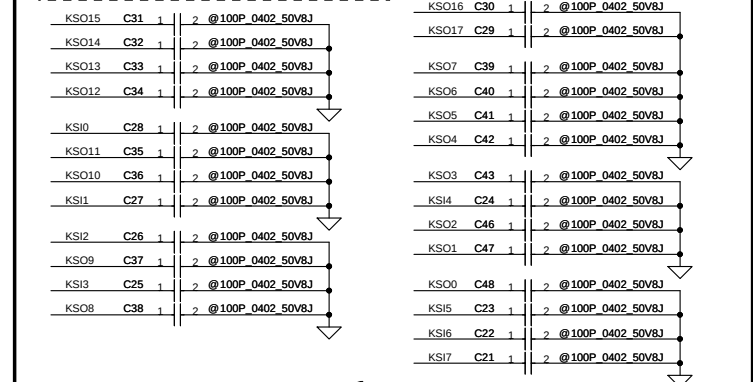
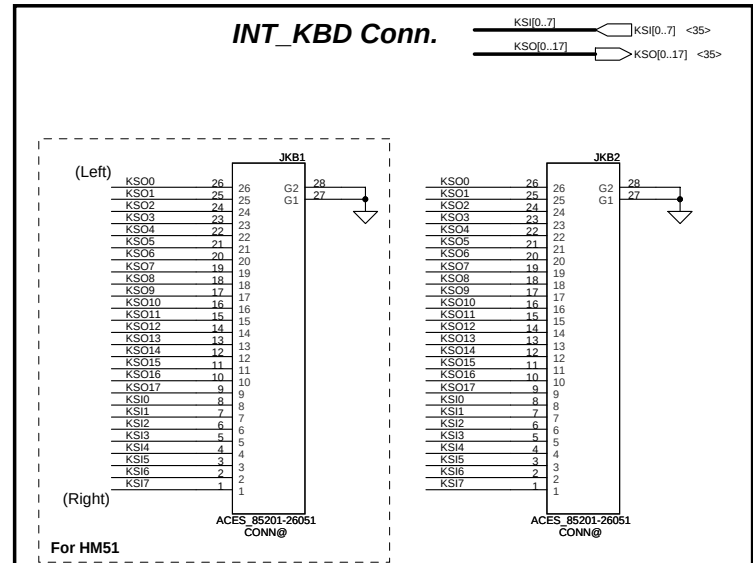
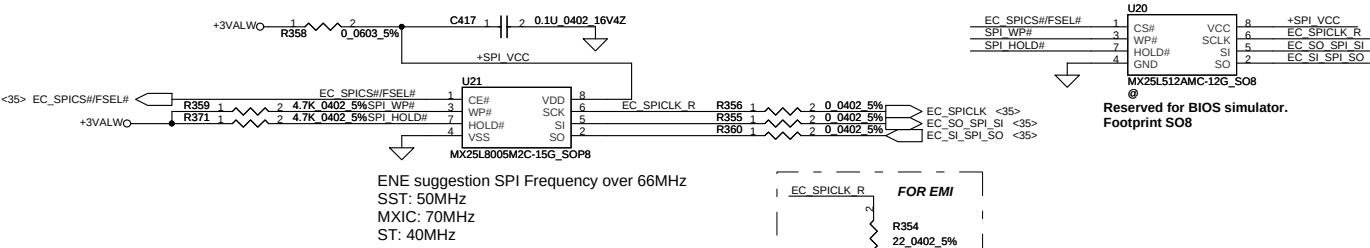
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



USB CONN.

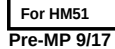


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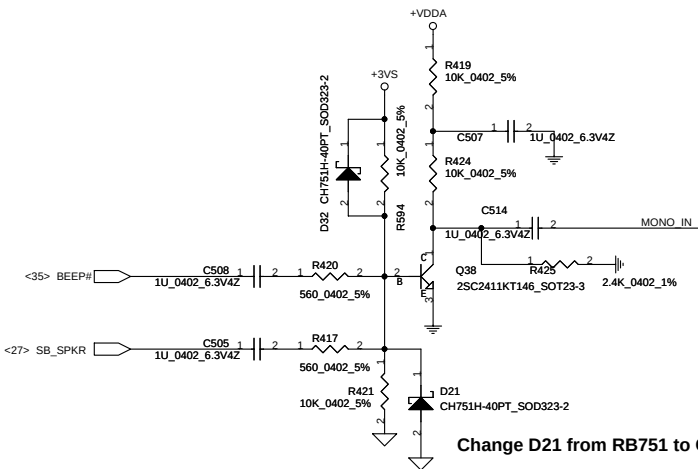


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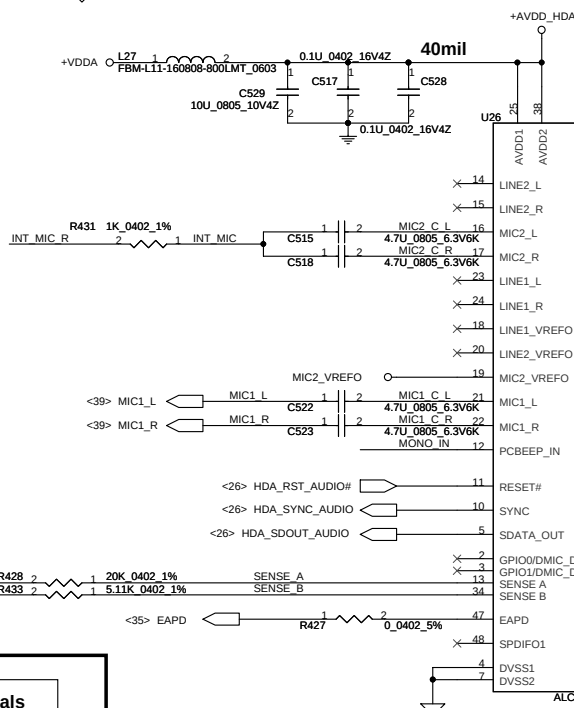
ON/OFF switch



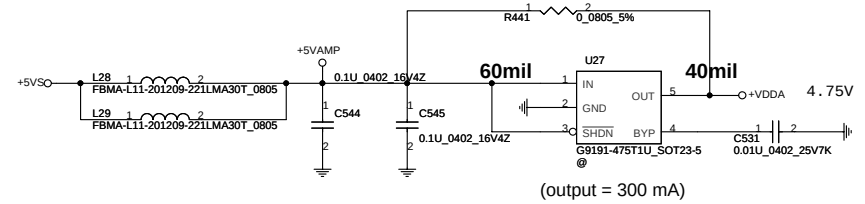
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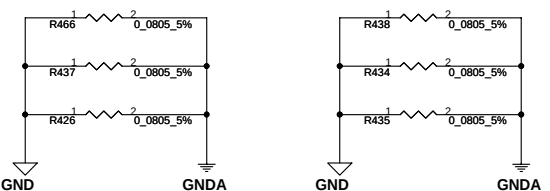
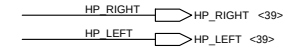
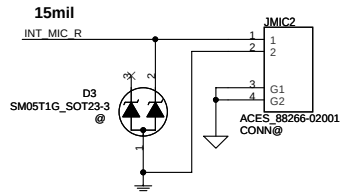
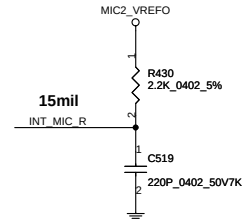
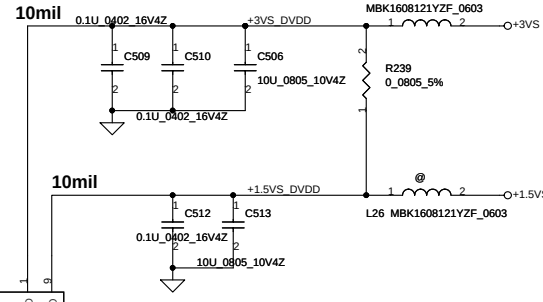
Change D21 from RB751 to CH751



HD Audio Codec

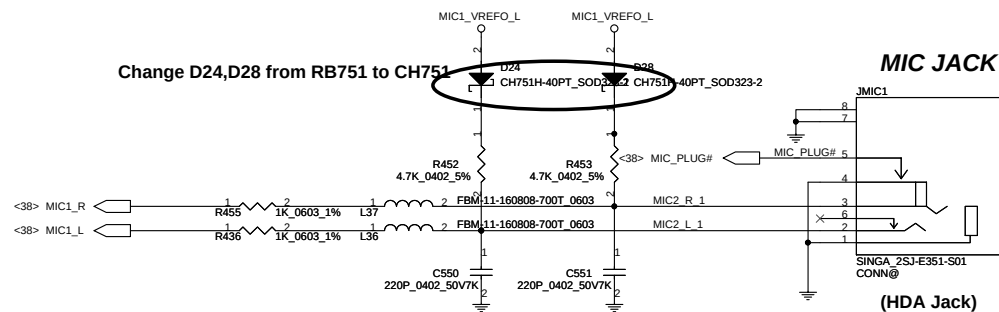
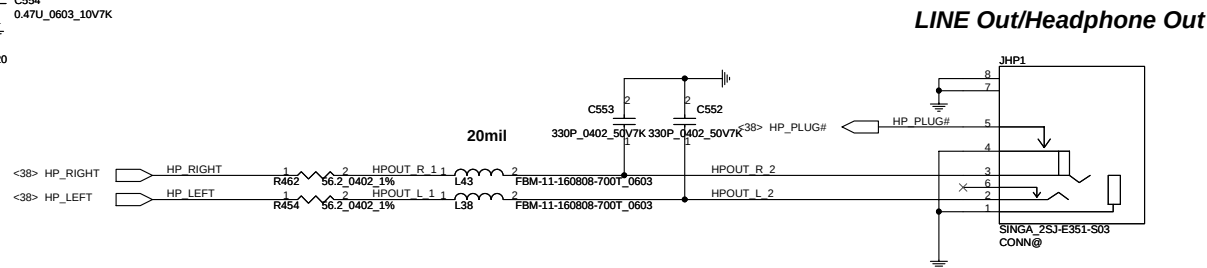
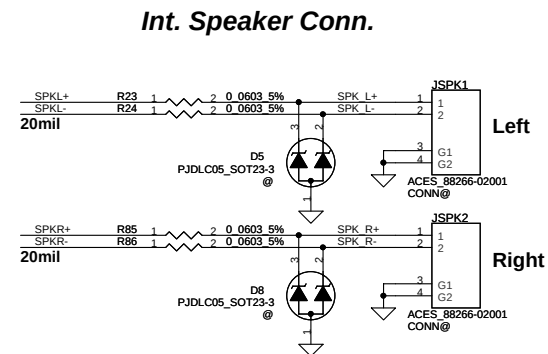
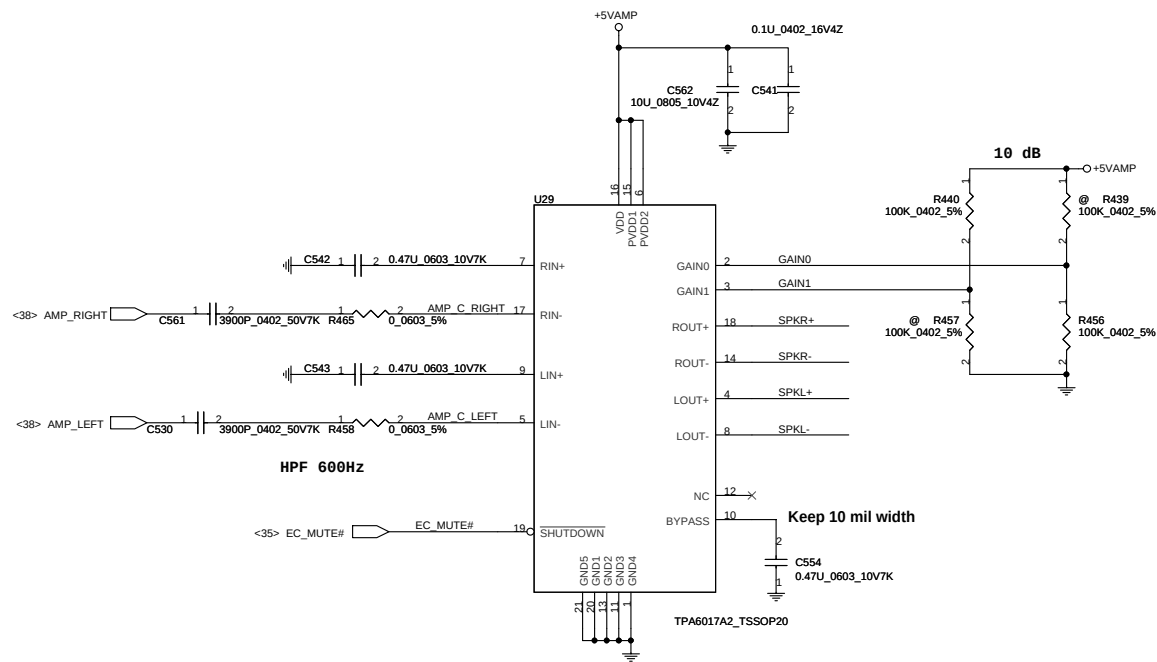


(output = 300 mA)



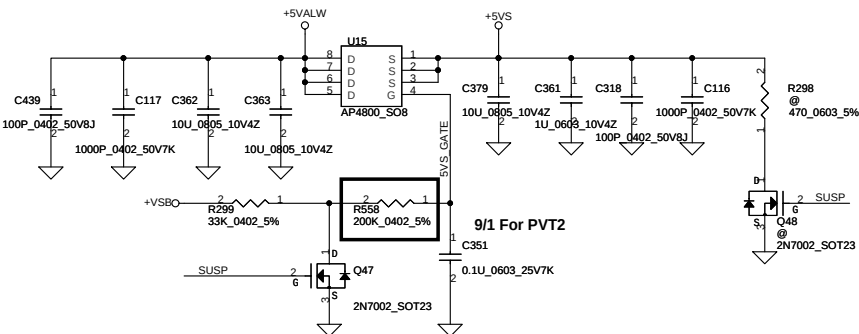
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-B (PIN 21, 22)
	20K	
	10K	
	5.1K	
SENSE B	39.2K	PORT-H (PIN 32,33)
	20K	
	10K	
	5.1K	

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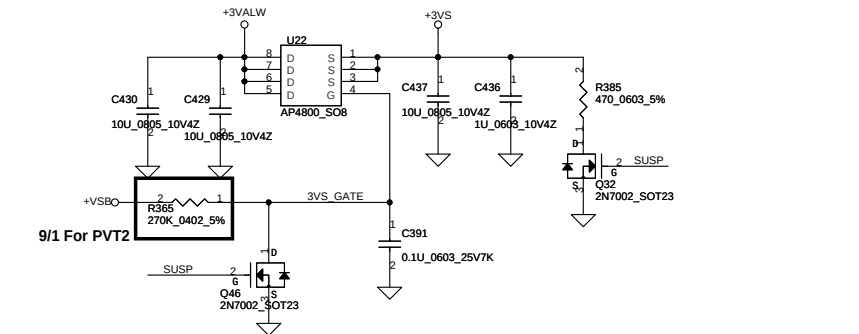


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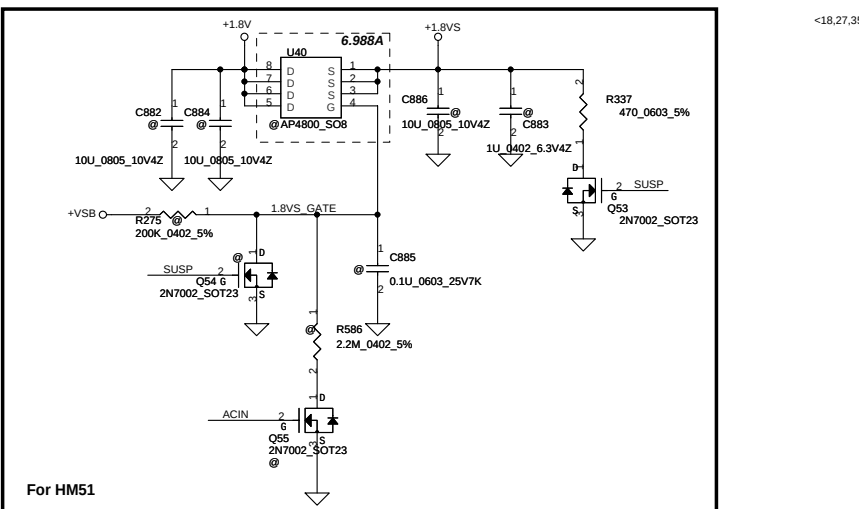
+5VALW TO +5VS



+3VALW TO +3VS



+1.8V to +1.8VS

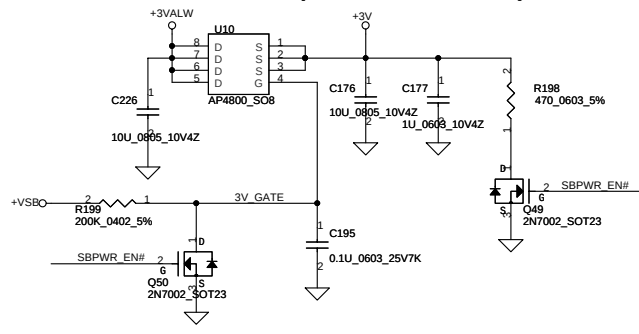


For HM51

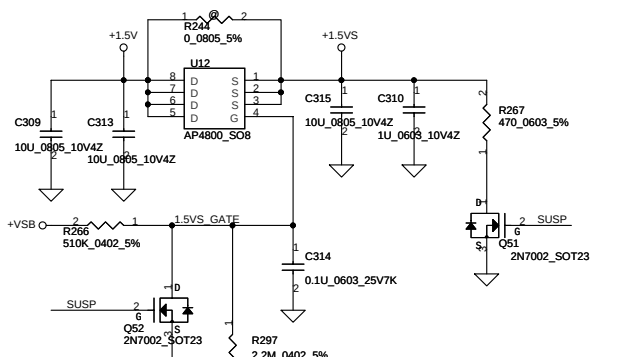
Pre-MP 9/17



+3VALW TO +3V_SB(ICH8M AUX Power)

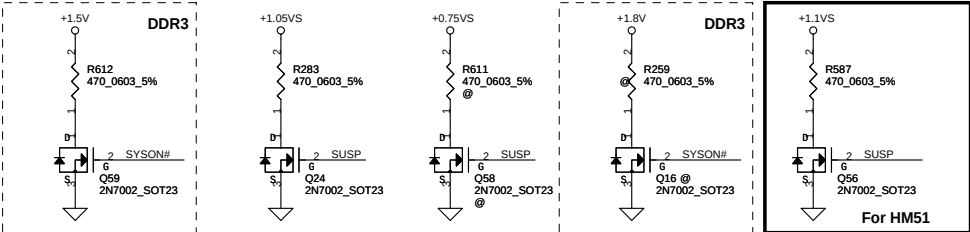
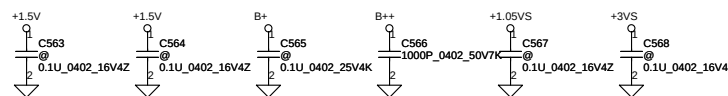


+1.5V to +1.5VS

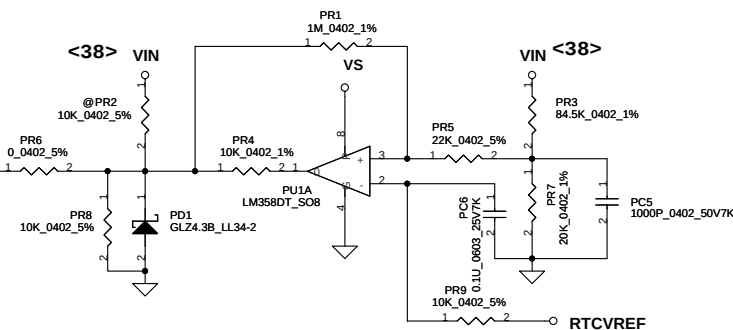
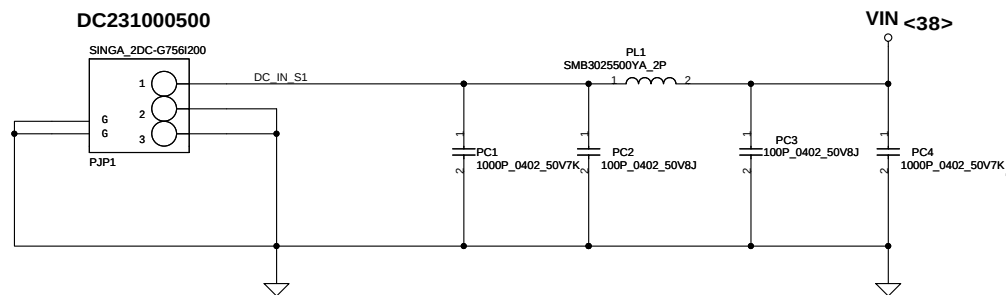


<18,27,35,41,44> ACIN

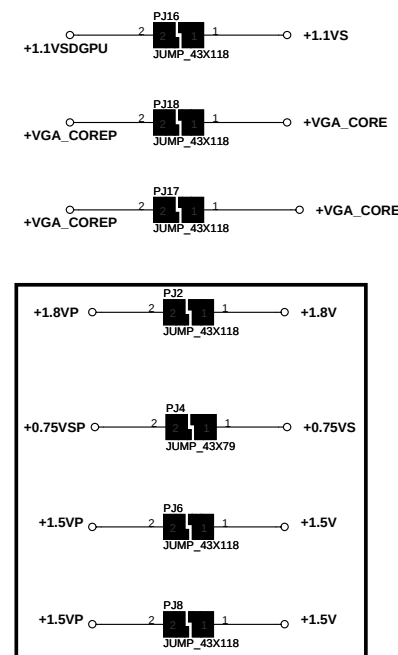
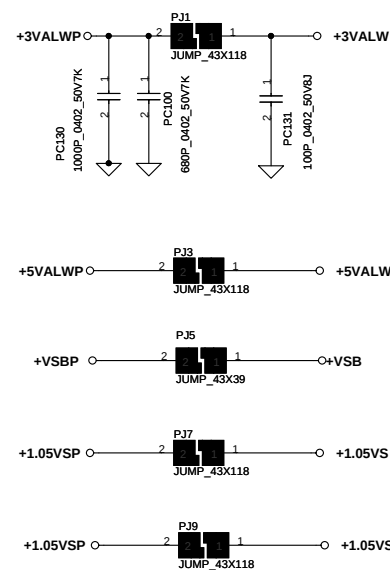
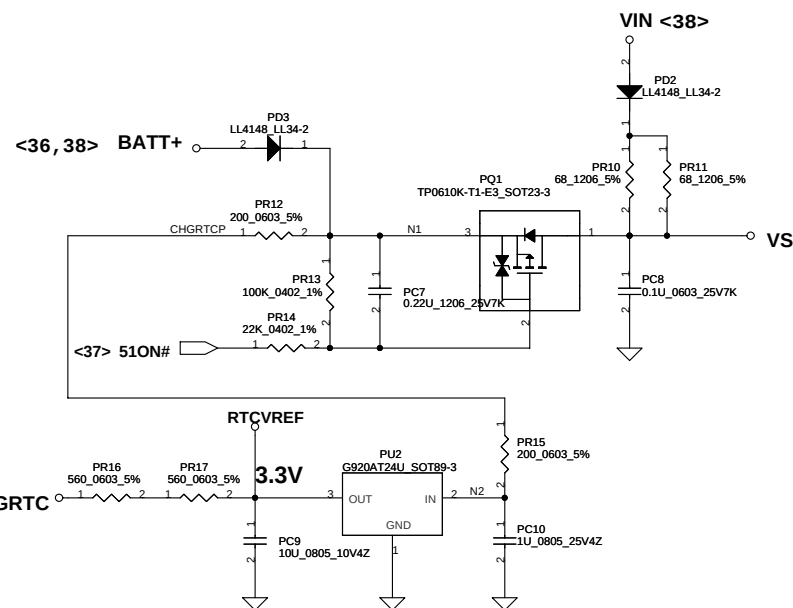
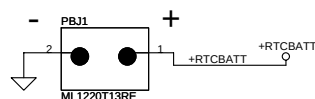
Reserve for EMI request



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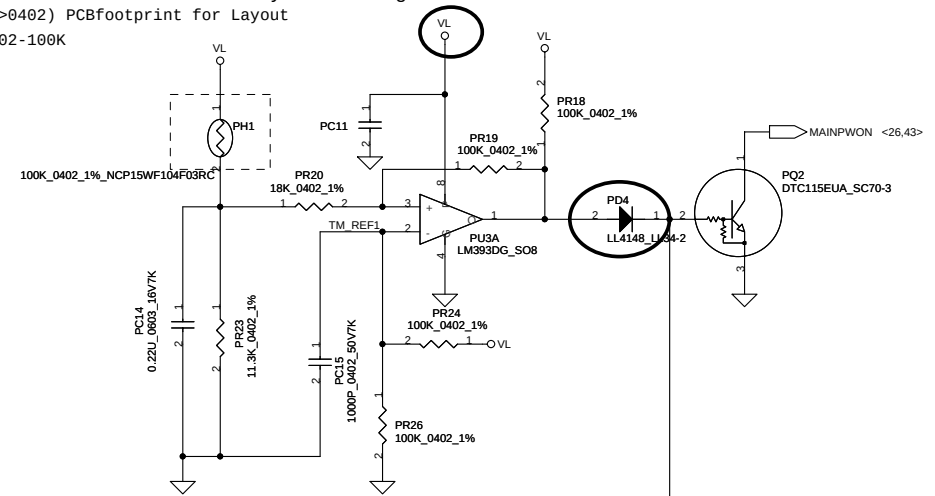
Vin Dectector				
	Min.	Typ	Max.	
H-->L	16.976V	17.525V	17.728V	
L-->H	17.430V	17.901V	18.384V	



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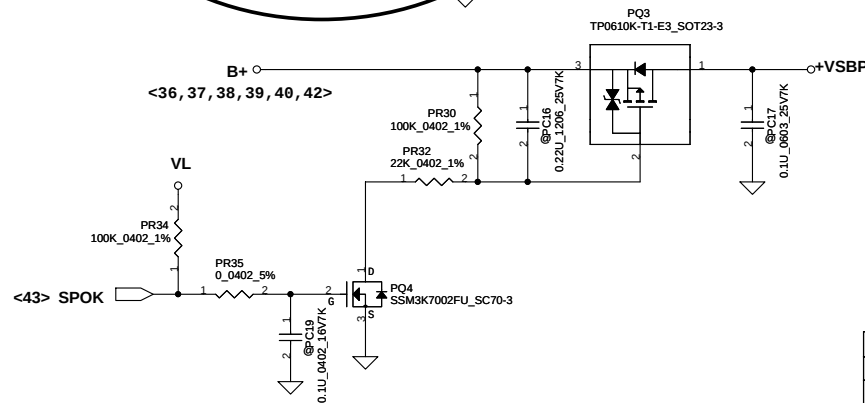
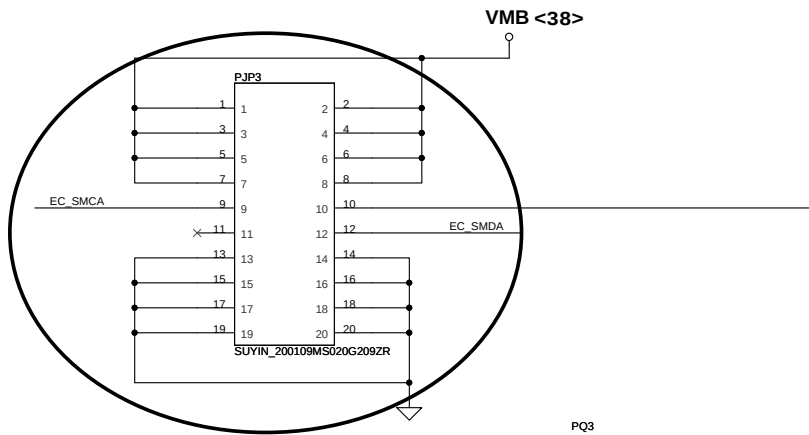
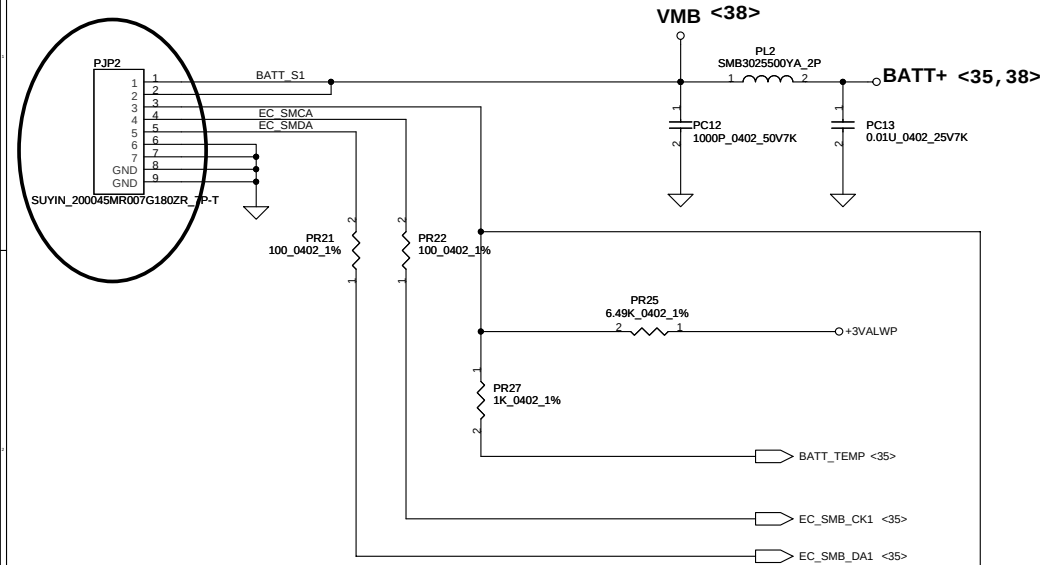
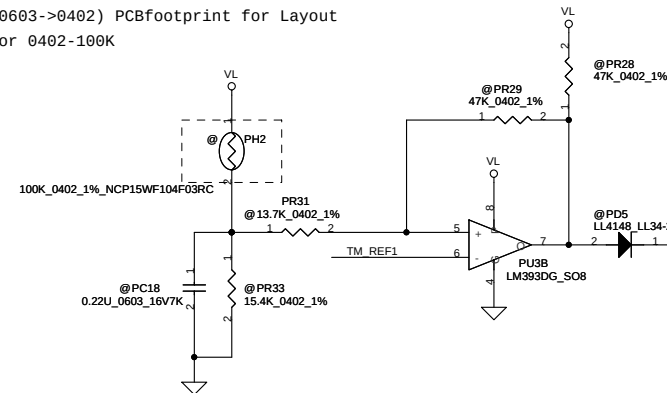
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

2009_08_06 (0603->0402) PCBfootprint for Layout
Change P/N for 0402-100K

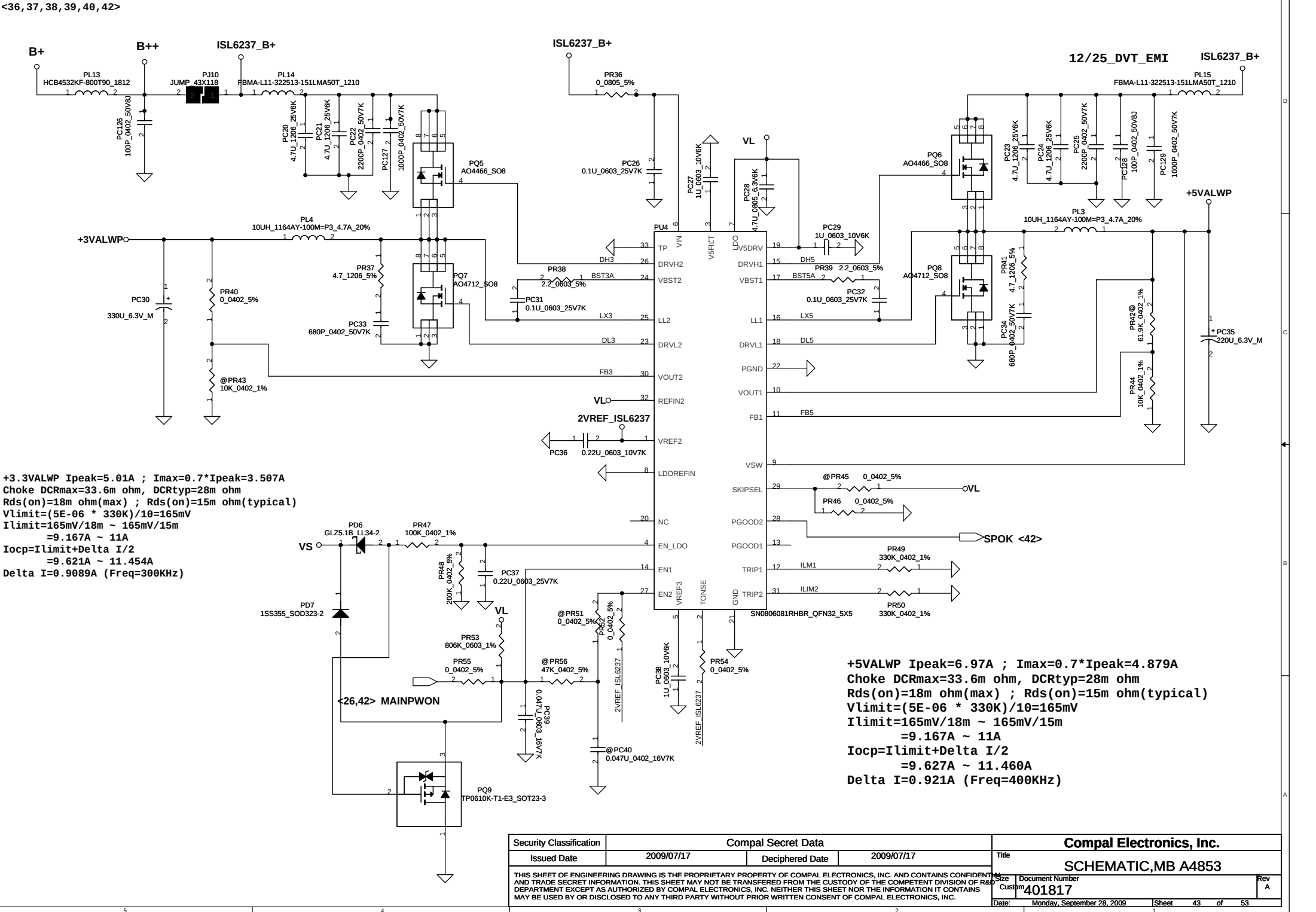


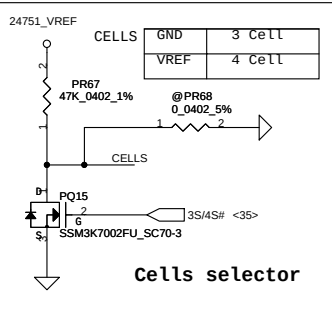
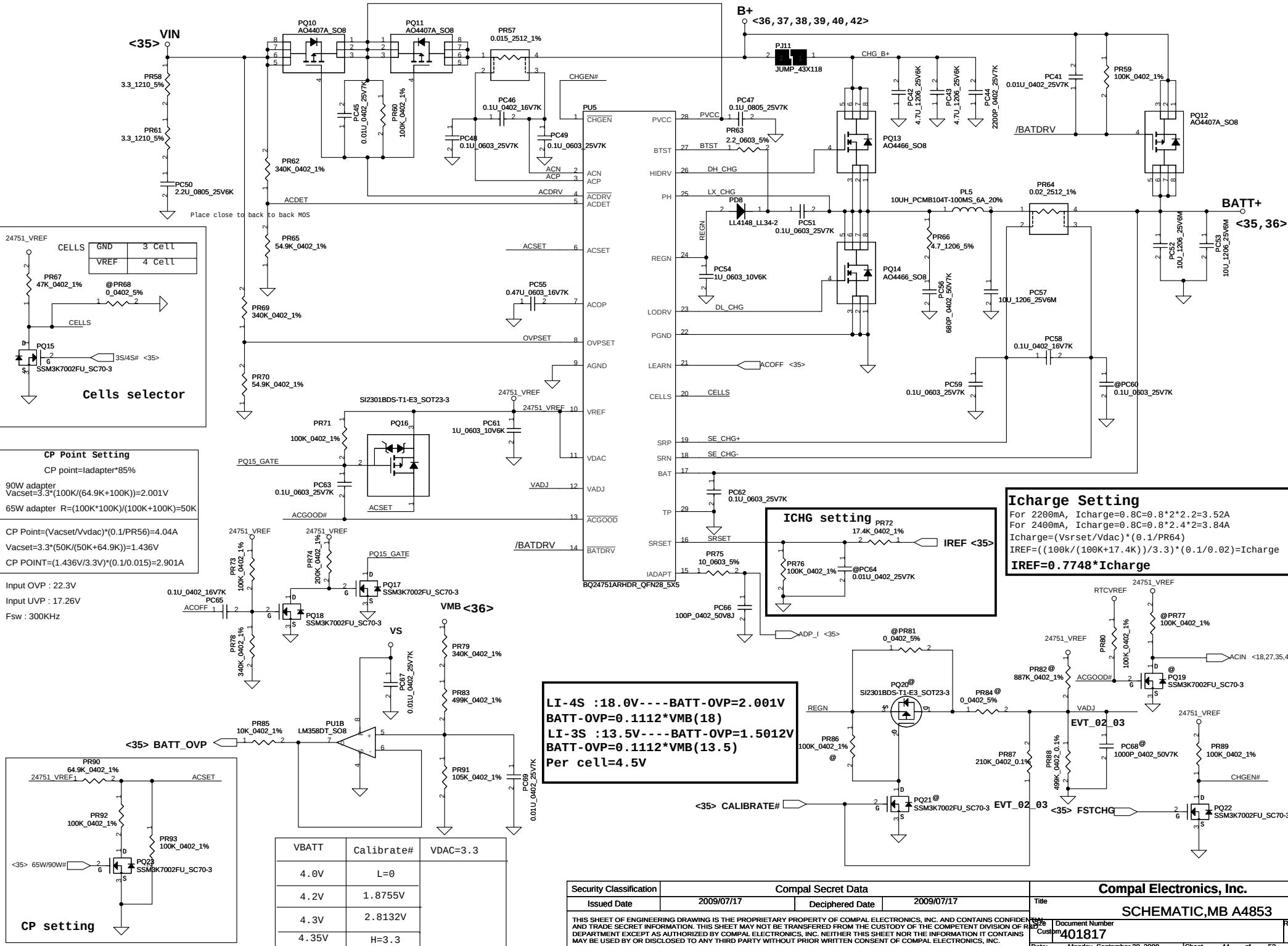
PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 70 degree C

2009_08_06 (0603->0402) PCBfootprint for Layout
Change P/N for 0402-100K



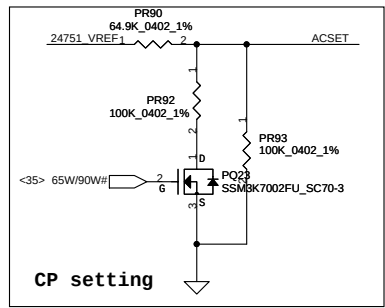
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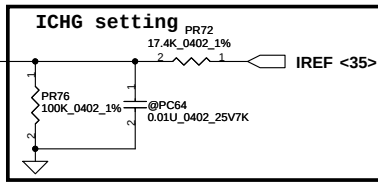
CP Point Setting
CP point=ladapter*85%
90W adapter
Vacset=3.3*(100K/(64.9K+100K))=2.001V
65W adapter R=(100K*100K)/(100K+100K)=50K
CP Point=(Vacset/Vvdac)*(0.1/PR56)=4.04A
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

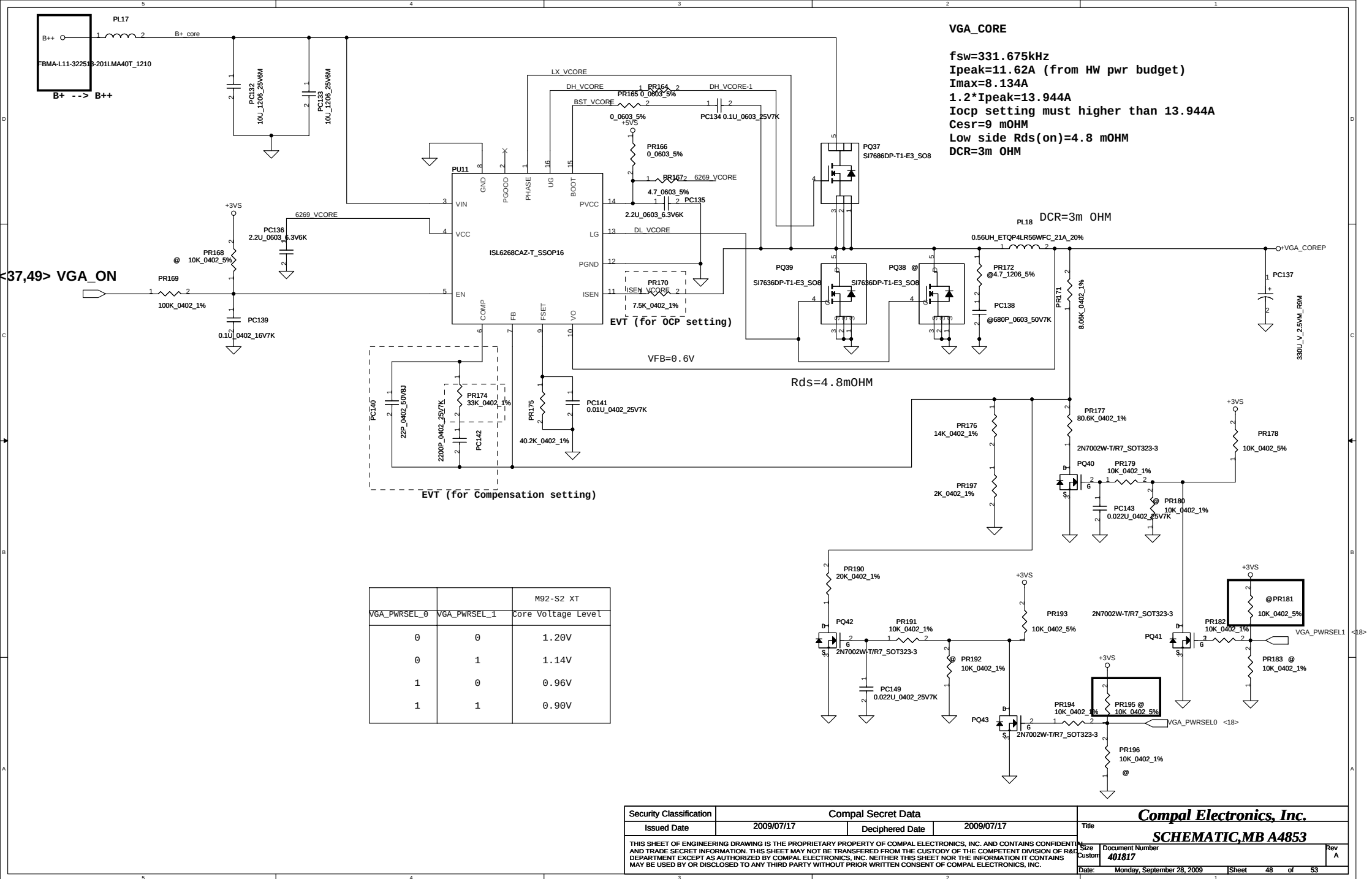


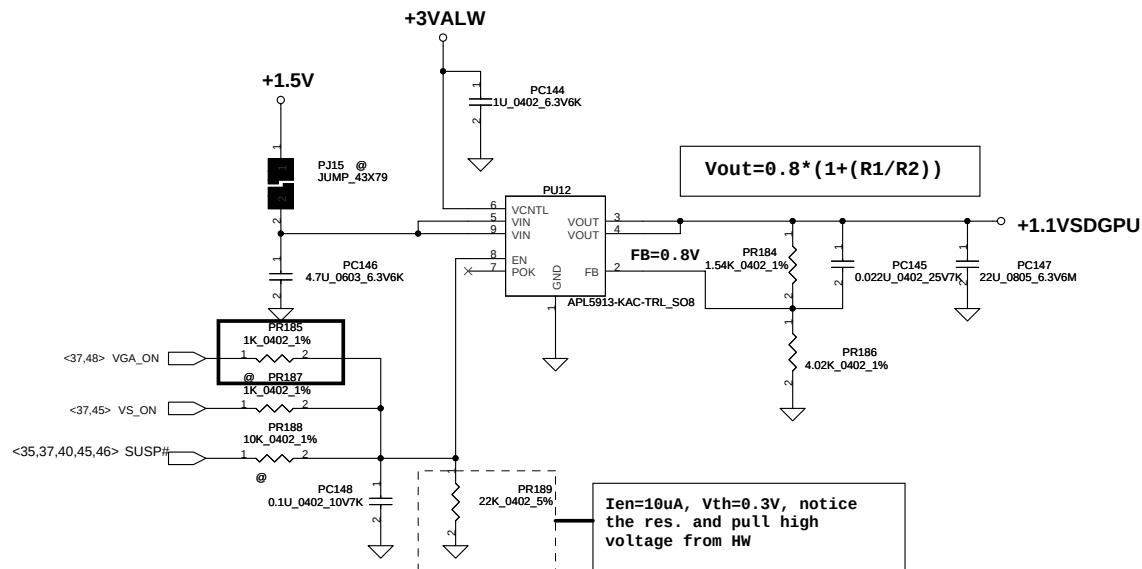
VBATT	Calibrate#	VDAC=3.3
4.0V	L=0	
4.2V	1.8755V	
4.3V	2.8132V	
4.35V	H=3.3	

LI-4S : 18.0V---BATT-OVP=2.001V
BATT-OVP=0.1112*VMB(18)
LI-3S : 13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB(13.5)
Per cell=4.5V



Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4*2=3.84A
Icharge=(Vsrset/Vdac)*(0.1/PR64)
IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge





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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_S0T23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%	0.2	38	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_S0T23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%	20081124	DVT
		39					
		40		+1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%			
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J	20081224	PVT
		40		+1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210			
20	POWER Solution	+3VALWP/+5VALWP RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT
		COMPAL ELECTRONICS					
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Item	Fixed Issue	Reason for change	Rev	PG #	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 (HCB4532KF-800T90_1812) Add PL 14 (FBMA-L11-322513-151LMA50T_1210) Add PL 15 (FBMA-L11-322513-151LMA50T_1210) Add PC126 (100P_0402_50V8J) Add PC128 (100P_0402_50V8J) Add PC129 (1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 (100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT

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8/21 For Change DDR3

- 1. P.40 Add R612, Q59 ; Unstuff R244 ; Remove R260, R253, Q13, Q14 ; stuff C309, C313, C315, C310, C314, R266, Q52, Q51, R267, U12 for +1.5V
- 2. P.40 Unstuff R611, Q58 for +0.75VS ; Add J3 for +1.8V ;
- 3. P.37 Unstuff R609, R610 ; Add R608, R606, R607, D33, U42, Q57 for DDR3
- 4. P.23 Unstuff R411, D20 ; Add R613 for BK0FF#
- 5. P.25 Unstuff U8, R83 ; Add R614 for PCI_RST#

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- 1. P.22 Unstuff R544, R545 for No HDMI Audio Function
- 2. P.40 Change R558 120K ohm as 200K ohm ; Change R200K ohm as 270K ohm

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- 1. P.40 Unstuff C882, C883, C884, C885, C886, R275, Q54, U40 for 1.8VS
- 2. P.31 Change C81, C82 27pF as 33pF for Xtal 25MHz(TXC suggest value)
- 3. P.26 Change C163, C164 18pF as 15pF for Xtal 32.768kHz (TXC suggest value)
- 4. P.37 Unstuff C407, C880, C881, R560, D30
- 5. P.41 Unstuff R580, U41
- 6. P.35 Change R273 8.2k ohm as 18k ohm for Board ID

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